

PCB Number: 17513

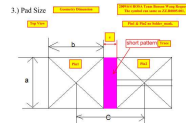
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0805 封装尺寸 / 0402 封装尺寸 /
0603 封装尺寸 / 1206 封装尺寸

封装尺寸与功率关系: 封装尺寸与封装的功率关系

0201 1/20W	0402=1.0mmx0.5mm
0402 1/16W	0603=1.6mmx0.8mm
0603 1/10W	0805=2.0mmx1.2mm
0805 1/8W	1206=3.2mmx1.6mm
1206 1/4W	1210=3.2mmx2.5mm
	1812=4.5mmx3.2mm
	2225=5.6mmx6.5mm



Distance (mm)	a	b	c	d
0402	1.6	0.8	0.8	0.8
0603	1.6	0.8	0.8	0.8
0805	1.6	0.8	0.8	0.8

Size Current
Short-PAD:
0402=ZZ.00PAD.M11=0.65A
0603=ZZ.00PAD.M21=0.875A
0805=ZZ.00PAD.M31=1.375A

TEST CONDITION FOR JUMPER (0W)

Item	WR12	WR08	WR06	WR04
Power Rating At 70°C	1/4W	1/8W	1/10W	1/16W
Resistance			MAX.50mW	
Rated Current	2A	1.5A	1A	1A
Peak Current	5A	3.5A	3A	1.5A
Operating Temperature		-55~155°C		

Design note:

10KR3	10K	R	3		
	value=10K	resistor	Size=0603		
SCD1U10V2	S	C	D1U	10V	2
	type=0603	capacitor	value=0.10	Withstand voltage=10V	Size=0402

BOM Configuration

(R):Unmount	(X):For debug
(IRMT):For IRMT control	(XDP):For XDP debug
(Nuvoton):Mount for Nuvoton TPM	
(Infineon):Mount for Infineon TPM	
(ST):Mount for st TPM	
(A710):For USB Charger / PS2 / On Board Function Key / Smart Power On / Board ID	(V330):For Non-USB Charger / Non-PS2 / Daughter Board Function Key / Non-Smart Power On / Board ID

```
Build Net==>
(Part Value):'{Value}!''{Part Number}'
(PCB Footprint):'{PCB Footprint}!''{PCB Footprint}'
' '{Value}!''{Part Number}' ' '{PCB Footprint}!''{PCB Footprint}'
```

```
Build BOM==>
#Reference\tPart Number\tSymbol\tGeometry\tF7\tFIN1\tFIN1
{Reference}\t{Part Number}\t{Value}\t{PCB Footprint}\t{F7}\t{FIN1}\t{FIN1}
{Reference}\tPart Number\tSymbol\tGeometry\tF7\tFIN1\tFIN1\t{Reference}\t{Part Number}\t{Value}\t{PCB Footprint}\t{F7}\t{FIN1}\t{FIN1}
```

```
Build VRT==>
Item Number\tReference\tCore Design\tBOM1\tValue\tDescription
{Item}\t{Reference}\t{Part Number}\t{F7}\t{Value}\t{Description}
```

```
Build OLE File==>
1. 先删除所有的DSN檔案，並且將要用的元件複製起來(如果是晶片組的話，只要其中一個即可)。
2. File->New->Design->將元件貼到Schematic的Page1，貼上之後會在Design Cache裡面出現一個*.OLE或者*.DSN檔案。
3. New->Library->Design Cache->*.OLE檔案，檔案拖到Library。
4. 在Library的*.OLE檔案，打開其他的子元件(View->Package)
5. 將之儲存(Save)即可。
6. 將*.OLE檔案Symbol team即可建立元件。
```

BD Information:

T=1.6 +/-0.1MM 6layers

L*W=228mmX 194mm

How to option FUSE

FUSE calculate Current:AI(A)

FUSE actual Current:A(A)

EXP calculate:

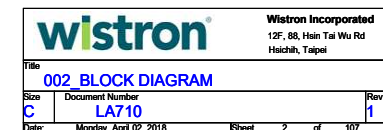
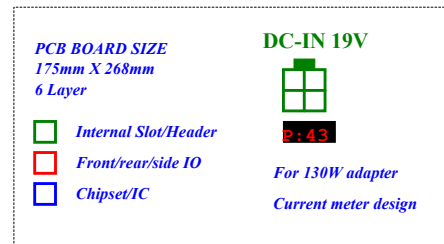
AI=X+0.8

1) A=AI+(/-0.1)

2) AI+0.1<=A<=AI+0.4

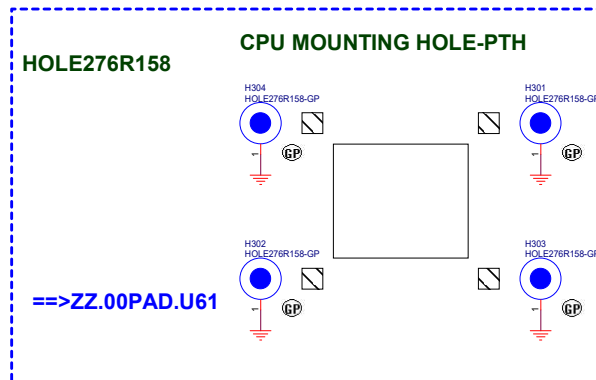
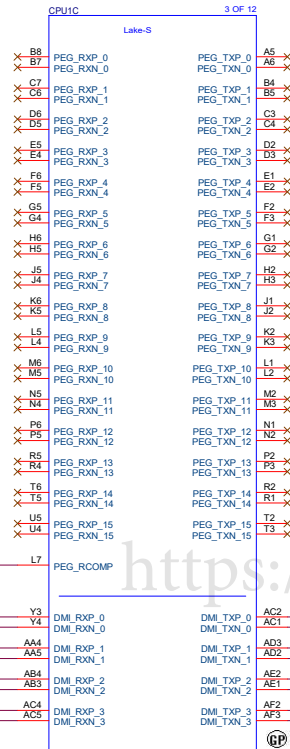
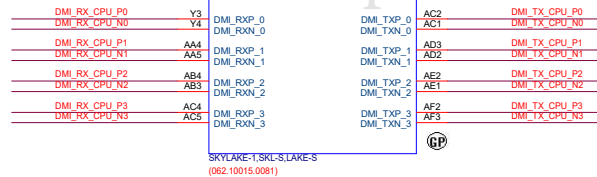
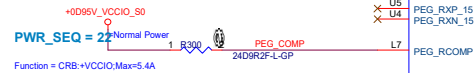
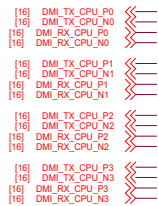
Find==>Part Reference=(C|R)[2-9]

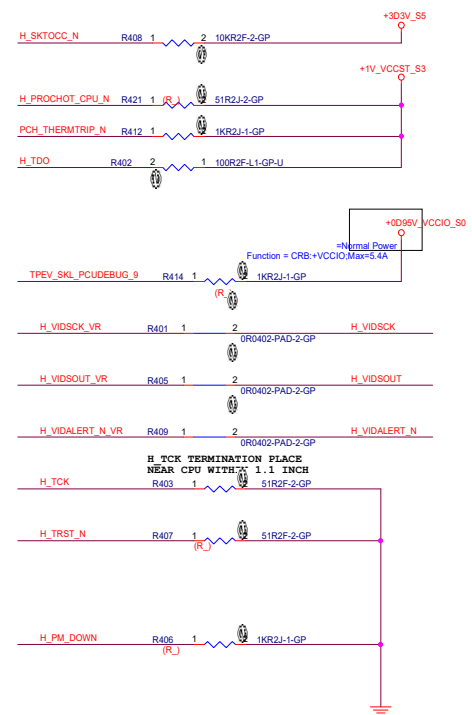
```
PCB Color==>
ET phase:Red
SDV phase:Blue
SIT/SVT phase:Green
```



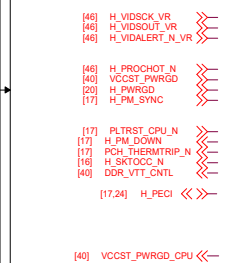
170828 Leon:Change CPU1 to 062.10015.0081 for SB

DMI

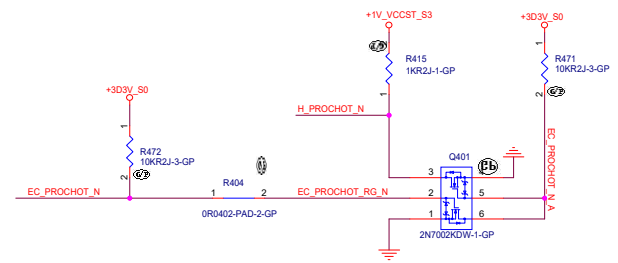




<https://vinafix.com>



PROCHOT CONTROL / EC SOLUTION



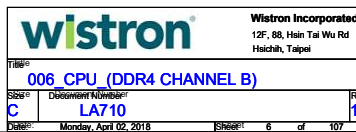
Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	<p>Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.</p> <p>Intel recommends placing test points on the board for CFG pins.</p> <ul style="list-style-type: none"> • CFG[0]: Stall reset sequence after PCIu PLL lock until de-asserted: <ul style="list-style-type: none"> — 1 = (Default) Normal Operation; No stall. — 0 = Stall. • CFG[1]: Reserved configuration lane. • CFG[2]: PCI Express* Static x16 Lane Numbering Reversal. <ul style="list-style-type: none"> — 1 = Normal operation — 0 = Lane numbers reversed. • CFG[3]: Reserved configuration lane. • CFG[4]: eDP* enable: <ul style="list-style-type: none"> — 1 = Disabled. — 0 = Enabled. • CFG[6:5]: PCI Express* Bifurcation <ul style="list-style-type: none"> — 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved — 10 = 2 x8 PCI Express* — 11 = 1 x16 PCI Express* • CFG[7]: PEG Training: <ul style="list-style-type: none"> — 1 = (default) PEG Train immediately following RESET# de assertion. — 0 = PEG Wait for BIOS for training. • CFG[19:8]: Reserved configuration lanes. 	I	GTL	SE	All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.

CHANNEL A DIMM0

170828 Leon:Change CPU1 to 062.10015.0081 for SB

CPU1A			1 OF 12		
CPU1A			Lake-S		
(11) M_A_DQ0	AE38	DDR0_DQ_0/DDR0_DQ_0	DDR0_CK0_0	AW18	M_A_CLK0
(11) M_A_DQ1	AE37	DDR0_DQ_1/DDR0_DQ_1	DDR0_CK0_1	AW18	M_A_CLK0
(11) M_A_DQ2	AG38	DDR0_DQ_2/DDR0_DQ_2	DDR0_CK0_2	AW17	M_A_CLK1
(11) M_A_DQ3	AG37	DDR0_DQ_3/DDR0_DQ_3	DDR0_CK0_3	AW17	M_A_CLK1
(11) M_A_DQ4	AE39	DDR0_DQ_4/DDR0_DQ_4	DDR0_CK0_4	AW18	M_A_CLK1
(11) M_A_DQ5	AE40	DDR0_DQ_5/DDR0_DQ_5	DDR0_CK0_5	AW18	M_A_CLK1
(11) M_A_DQ6	AG39	DDR0_DQ_6/DDR0_DQ_6	DDR0_CK0_6	AW18	M_A_CLK1
(11) M_A_DQ7	AG40	DDR0_DQ_7/DDR0_DQ_7	DDR0_CK0_7	AW18	M_A_CLK1
(11) M_A_DQ8	AE38	DDR0_DQ_8/DDR0_DQ_8	DDR0_CK0_8	AW18	M_A_CLK1
(11) M_A_DQ9	AE37	DDR0_DQ_9/DDR0_DQ_9	DDR0_CK0_9	AW18	M_A_CLK1
(11) M_A_DQ10	AG38	DDR0_DQ_10/DDR0_DQ_10	DDR0_CK0_10	AW17	M_A_CLK1
(11) M_A_DQ11	AG37	DDR0_DQ_11/DDR0_DQ_11	DDR0_CK0_11	AW17	M_A_CLK1
(11) M_A_DQ12	AE39	DDR0_DQ_12/DDR0_DQ_12	DDR0_CK0_12	AW18	M_A_CLK1
(11) M_A_DQ13	AE40	DDR0_DQ_13/DDR0_DQ_13	DDR0_CK0_13	AW18	M_A_CLK1
(11) M_A_DQ14	AG39	DDR0_DQ_14/DDR0_DQ_14	DDR0_CK0_14	AW18	M_A_CLK1
(11) M_A_DQ15	AG40	DDR0_DQ_15/DDR0_DQ_15	DDR0_CK0_15	AW18	M_A_CLK1
(11) M_A_DQ16	AE38	DDR0_DQ_16/DDR0_DQ_16	DDR0_CK0_16	AW18	M_A_CLK1
(11) M_A_DQ17	AE37	DDR0_DQ_17/DDR0_DQ_17	DDR0_CK0_17	AW18	M_A_CLK1
(11) M_A_DQ18	AG38	DDR0_DQ_18/DDR0_DQ_18	DDR0_CK0_18	AW17	M_A_CLK1
(11) M_A_DQ19	AG37	DDR0_DQ_19/DDR0_DQ_19	DDR0_CK0_19	AW17	M_A_CLK1
(11) M_A_DQ20	AE39	DDR0_DQ_20/DDR0_DQ_20	DDR0_CK0_20	AW18	M_A_CLK1
(11) M_A_DQ21	AE40	DDR0_DQ_21/DDR0_DQ_21	DDR0_CK0_21	AW18	M_A_CLK1
(11) M_A_DQ22	AG39	DDR0_DQ_22/DDR0_DQ_22	DDR0_CK0_22	AW18	M_A_CLK1
(11) M_A_DQ23	AG40	DDR0_DQ_23/DDR0_DQ_23	DDR0_CK0_23	AW18	M_A_CLK1
(11) M_A_DQ24	AE38	DDR0_DQ_24/DDR0_DQ_24	DDR0_CK0_24	AW18	M_A_CLK1
(11) M_A_DQ25	AE37	DDR0_DQ_25/DDR0_DQ_25	DDR0_CK0_25	AW18	M_A_CLK1
(11) M_A_DQ26	AG38	DDR0_DQ_26/DDR0_DQ_26	DDR0_CK0_26	AW17	M_A_CLK1
(11) M_A_DQ27	AG37	DDR0_DQ_27/DDR0_DQ_27	DDR0_CK0_27	AW17	M_A_CLK1
(11) M_A_DQ28	AE39	DDR0_DQ_28/DDR0_DQ_28	DDR0_CK0_28	AW18	M_A_CLK1
(11) M_A_DQ29	AE40	DDR0_DQ_29/DDR0_DQ_29	DDR0_CK0_29	AW18	M_A_CLK1
(11) M_A_DQ30	AG39	DDR0_DQ_30/DDR0_DQ_30	DDR0_CK0_30	AW18	M_A_CLK1
(11) M_A_DQ31	AG40	DDR0_DQ_31/DDR0_DQ_31	DDR0_CK0_31	AW18	M_A_CLK1
(11) M_A_DQ32	AE38	DDR0_DQ_32/DDR0_DQ_32	DDR0_CK0_32	AW18	M_A_CLK1
(11) M_A_DQ33	AE37	DDR0_DQ_33/DDR0_DQ_33	DDR0_CK0_33	AW18	M_A_CLK1
(11) M_A_DQ34	AG38	DDR0_DQ_34/DDR0_DQ_34	DDR0_CK0_34	AW17	M_A_CLK1
(11) M_A_DQ35	AG37	DDR0_DQ_35/DDR0_DQ_35	DDR0_CK0_35	AW17	M_A_CLK1
(11) M_A_DQ36	AE39	DDR0_DQ_36/DDR0_DQ_36	DDR0_CK0_36	AW18	M_A_CLK1
(11) M_A_DQ37	AE40	DDR0_DQ_37/DDR0_DQ_37	DDR0_CK0_37	AW18	M_A_CLK1
(11) M_A_DQ38	AG39	DDR0_DQ_38/DDR0_DQ_38	DDR0_CK0_38	AW18	M_A_CLK1
(11) M_A_DQ39	AG40	DDR0_DQ_39/DDR0_DQ_39	DDR0_CK0_39	AW18	M_A_CLK1
(11) M_A_DQ40	AE38	DDR0_DQ_40/DDR0_DQ_40	DDR0_CK0_40	AW18	M_A_CLK1
(11) M_A_DQ41	AE37	DDR0_DQ_41/DDR0_DQ_41	DDR0_CK0_41	AW18	M_A_CLK1
(11) M_A_DQ42	AG38	DDR0_DQ_42/DDR0_DQ_42	DDR0_CK0_42	AW17	M_A_CLK1
(11) M_A_DQ43	AG37	DDR0_DQ_43/DDR0_DQ_43	DDR0_CK0_43	AW17	M_A_CLK1
(11) M_A_DQ44	AE39	DDR0_DQ_44/DDR0_DQ_44	DDR0_CK0_44	AW18	M_A_CLK1
(11) M_A_DQ45	AE40	DDR0_DQ_45/DDR0_DQ_45	DDR0_CK0_45	AW18	M_A_CLK1
(11) M_A_DQ46	AG39	DDR0_DQ_46/DDR0_DQ_46	DDR0_CK0_46	AW18	M_A_CLK1
(11) M_A_DQ47	AG40	DDR0_DQ_47/DDR0_DQ_47	DDR0_CK0_47	AW18	M_A_CLK1
(11) M_A_DQ48	AE38	DDR0_DQ_48/DDR0_DQ_48	DDR0_CK0_48	AW18	M_A_CLK1
(11) M_A_DQ49	AE37	DDR0_DQ_49/DDR0_DQ_49	DDR0_CK0_49	AW18	M_A_CLK1
(11) M_A_DQ50	AG38	DDR0_DQ_50/DDR0_DQ_50	DDR0_CK0_50	AW17	M_A_CLK1
(11) M_A_DQ51	AG37	DDR0_DQ_51/DDR0_DQ_51	DDR0_CK0_51	AW17	M_A_CLK1
(11) M_A_DQ52	AE39	DDR0_DQ_52/DDR0_DQ_52	DDR0_CK0_52	AW18	M_A_CLK1
(11) M_A_DQ53	AE40	DDR0_DQ_53/DDR0_DQ_53	DDR0_CK0_53	AW18	M_A_CLK1
(11) M_A_DQ54	AG39	DDR0_DQ_54/DDR0_DQ_54	DDR0_CK0_54	AW18	M_A_CLK1
(11) M_A_DQ55	AG40	DDR0_DQ_55/DDR0_DQ_55	DDR0_CK0_55	AW18	M_A_CLK1
(11) M_A_DQ56	AE38	DDR0_DQ_56/DDR0_DQ_56	DDR0_CK0_56	AW18	M_A_CLK1
(11) M_A_DQ57	AE37	DDR0_DQ_57/DDR0_DQ_57	DDR0_CK0_57	AW18	M_A_CLK1
(11) M_A_DQ58	AG38	DDR0_DQ_58/DDR0_DQ_58	DDR0_CK0_58	AW17	M_A_CLK1
(11) M_A_DQ59	AG37	DDR0_DQ_59/DDR0_DQ_59	DDR0_CK0_59	AW17	M_A_CLK1
(11) M_A_DQ60	AE39	DDR0_DQ_60/DDR0_DQ_60	DDR0_CK0_60	AW18	M_A_CLK1
(11) M_A_DQ61	AE40	DDR0_DQ_61/DDR0_DQ_61	DDR0_CK0_61	AW18	M_A_CLK1
(11) M_A_DQ62	AG39	DDR0_DQ_62/DDR0_DQ_62	DDR0_CK0_62	AW18	M_A_CLK1
(11) M_A_DQ63	AG40	DDR0_DQ_63/DDR0_DQ_63	DDR0_CK0_63	AW18	M_A_CLK1
(11) M_A_DQ64	AE38	DDR0_DQ_64/DDR0_DQ_64	DDR0_CK0_64	AW18	M_A_CLK1
(11) M_A_DQ65	AE37	DDR0_DQ_65/DDR0_DQ_65	DDR0_CK0_65	AW18	M_A_CLK1
(11) M_A_DQ66	AG38	DDR0_DQ_66/DDR0_DQ_66	DDR0_CK0_66	AW17	M_A_CLK1
(11) M_A_DQ67	AG37	DDR0_DQ_67/DDR0_DQ_67	DDR0_CK0_67	AW17	M_A_CLK1
(11) M_A_DQ68	AE39	DDR0_DQ_68/DDR0_DQ_68	DDR0_CK0_68	AW18	M_A_CLK1
(11) M_A_DQ69	AE40	DDR0_DQ_69/DDR0_DQ_69	DDR0_CK0_69	AW18	M_A_CLK1
(11) M_A_DQ70	AG39	DDR0_DQ_70/DDR0_DQ_70	DDR0_CK0_70	AW18	M_A_CLK1
(11) M_A_DQ71	AG40	DDR0_DQ_71/DDR0_DQ_71	DDR0_CK0_71	AW18	M_A_CLK1
(11) M_A_DQ72	AE38	DDR0_DQ_72/DDR0_DQ_72	DDR0_CK0_72	AW18	M_A_CLK1
(11) M_A_DQ73	AE37	DDR0_DQ_73/DDR0_DQ_73	DDR0_CK0_73	AW18	M_A_CLK1
(11) M_A_DQ74	AG38	DDR0_DQ_74/DDR0_DQ_74	DDR0_CK0_74	AW17	M_A_CLK1
(11) M_A_DQ75	AG37	DDR0_DQ_75/DDR0_DQ_75	DDR0_CK0_75	AW17	M_A_CLK1
(11) M_A_DQ76	AE39	DDR0_DQ_76/DDR0_DQ_76	DDR0_CK0_76	AW18	M_A_CLK1
(11) M_A_DQ77	AE40	DDR0_DQ_77/DDR0_DQ_77	DDR0_CK0_77	AW18	M_A_CLK1
(11) M_A_DQ78	AG39	DDR0_DQ_78/DDR0_DQ_78	DDR0_CK0_78	AW18	M_A_CLK1
(11) M_A_DQ79	AG40	DDR0_DQ_79/DDR0_DQ_79	DDR0_CK0_79	AW18	M_A_CLK1
(11) M_A_DQ80	AE38	DDR0_DQ_80/DDR0_DQ_80	DDR0_CK0_80	AW18	M_A_CLK1
(11) M_A_DQ81	AE37	DDR0_DQ_81/DDR0_DQ_81	DDR0_CK0_81	AW18	M_A_CLK1
(11) M_A_DQ82	AG38	DDR0_DQ_82/DDR0_DQ_82	DDR0_CK0_82	AW17	M_A_CLK1
(11) M_A_DQ83	AG37	DDR0_DQ_83/DDR0_DQ_83	DDR0_CK0_83	AW17	M_A_CLK1
(11) M_A_DQ84	AE39	DDR0_DQ_84/DDR0_DQ_84	DDR0_CK0_84	AW18	M_A_CLK1
(11) M_A_DQ85	AE40	DDR0_DQ_85/DDR0_DQ_85	DDR0_CK0_85	AW18	M_A_CLK1
(11) M_A_DQ86	AG39	DDR0_DQ_86/DDR0_DQ_86	DDR0_CK0_86	AW18	M_A_CLK1
(11) M_A_DQ87	AG40	DDR0_DQ_87/DDR0_DQ_87	DDR0_CK0_87	AW18	M_A_CLK1
(11) M_A_DQ88	AE38	DDR0_DQ_88/DDR0_DQ_88	DDR0_CK0_88	AW18	M_A_CLK1
(11) M_A_DQ89	AE37	DDR0_DQ_89/DDR0_DQ_89	DDR0_CK0_89	AW18	M_A_CLK1
(11) M_A_DQ90	AG38	DDR0_DQ_90/DDR0_DQ_90	DDR0_CK0_90	AW17	M_A_CLK1
(11) M_A_DQ91	AG37	DDR0_DQ_91/DDR0_DQ_91	DDR0_CK0_91	AW17	M_A_CLK1
(11) M_A_DQ92	AE39	DDR0_DQ_92/DDR0_DQ_92	DDR0_CK0_92	AW18	M_A_CLK1
(11) M_A_DQ93	AE40	DDR0_DQ_93/DDR0_DQ_93	DDR0_CK0_93	AW18	M_A_CLK1
(11) M_A_DQ94	AG39	DDR0_DQ_94/DDR0_DQ_94	DDR0_CK0_94	AW18	M_A_CLK1
(11) M_A_DQ95	AG40	DDR0_DQ_95/DDR0_DQ_95	DDR0_CK0_95	AW18	M_A_CLK1
(11) M_A_DQ96	AE38	DDR0_DQ_96/DDR0_DQ_96	DDR0_CK0_96	AW18	M_A_CLK1
(11) M_A_DQ97	AE37	DDR0_DQ_97/DDR0_DQ_97	DDR0_CK0_97	AW18	M_A_CLK1
(11) M_A_DQ98	AG38	DDR0_DQ_98/DDR0_DQ_98	DDR0_CK0_98	AW17	M_A_CLK1
(11) M_A_DQ99	AG37	DDR0_DQ_99/DDR0_DQ_99	DDR0_CK0_99	AW17	M_A_CLK1
(11) M_A_DQ100	AE39	DDR0_DQ_100/DDR0_DQ_100	DDR0_CK0_100	AW18	M_A_CLK1
(11) M_A_DQ101	AE40	DDR0_DQ_101/DDR0_DQ_101	DDR0_CK0_101	AW18	M_A_CLK1
(11) M_A_DQ102	AG39	DDR0_DQ_102/DDR0_DQ_102	DDR0_CK0_102	AW18	M_A_CLK1
(11) M_A_DQ103	AG40	DDR0_DQ_103/DDR0_DQ_103	DDR0_CK0_103	AW18	M_A_CLK1
(11) M_A_DQ104	AE38	DDR0_DQ_104/DDR0_DQ_104	DDR0_CK0_104	AW18	M_A_CLK1
(11) M_A_DQ105	AE37	DDR0_DQ_105/DDR0_DQ_105	DDR0_CK0_105	AW18	M_A_CLK1
(11) M_A_DQ106	AG38	DDR0_DQ_106/DDR0_DQ_106	DDR0_CK0_106	AW17	M_A_CLK1
(11) M_A_DQ107	AG37	DDR0_DQ_107/DDR0_DQ_107	DDR0_CK0_107	AW17	M_A_CLK1
(11) M_A_DQ108	AE39	DDR0_DQ_108/DDR0_DQ_108	DDR0_CK0_108	AW18	M_A_CLK1
(11) M_A_DQ109	AE40	DDR0_DQ_109/DDR0_DQ_109	DDR0_CK0_109	AW18	M_A_CLK1
(11) M_A_DQ110	AG39	DDR0_DQ_110/DDR0_DQ_110	DDR0_CK0_110	AW18	M_A_CLK1
(11) M_A_DQ111	AG40	DDR0_DQ_111/DDR0_DQ_111	DDR0_CK0_111	AW18	M_A_CLK1
(11) M_A_DQ112	AE38	DDR0_DQ_112/DDR0_DQ_112	DDR0_CK0_112	AW18	M_A_CLK1
(11) M_A_DQ113	AE37	DDR0_DQ_113/DDR0_DQ_113	DDR0_CK0_113	AW18	M_A_CLK1
(11) M_A_DQ114	AG38	DDR0_DQ_114/DDR0_DQ_114	DDR0_CK0_114	AW17	M_A_CLK1
(11) M_A_DQ115	AG37	DDR0_DQ_115/DDR0_DQ_115	DDR0_CK0_115	AW17	M_A_CLK1
(11) M_A_DQ116	AE39	DDR0_DQ_116/DDR0_DQ_116	DDR0_CK0_116	AW18	M_A_CLK1
(11) M_A_DQ117	AE40	DDR0_DQ_117/DDR0_DQ_117	DDR0_CK0_117	AW18	M_A_CLK1
(11) M_A_DQ118	AG39	DDR0_DQ_118/DDR0_DQ_118	DDR0_CK0_118	AW18	M_A_CLK1
(11) M_A_DQ119	AG40	DDR0_DQ_119/DDR0_DQ_119	DDR0_CK0_119	AW18	M_A_CLK1
(11) M_A_DQ120	AE38	DDR0_DQ_120/DDR0_DQ_120	DDR0_CK0_120	AW18	M_A_CLK1
(11) M_A_DQ121	AE37	DDR0_DQ_121/DDR0_DQ_121	DDR0_CK0_121	AW18	M_A_CLK1
(11) M_A_DQ122	AG38	DDR0_DQ_122/DDR0_DQ_122	DDR0_CK0_122	AW17	M_A_CLK1
(11) M_A_DQ123	AG37	DDR0_DQ_123/DDR0_DQ_123	DDR0_CK0_123	AW17	M_A_CLK1
(11) M_A_DQ124	AE39	DDR0_DQ_124/DDR0_DQ_124	DDR0_CK0_124	AW18	M_A_CLK1
(11) M_A_DQ125	AE40	DDR0_DQ_125/DDR0_DQ_125	DDR0_CK0_125	AW18	M_A_CLK1
(11) M_A_DQ126	AG39	DDR0_DQ_126/DDR0_DQ_126	DDR0_CK0_126	AW18	M_A_CLK1
(11) M_A_DQ127	AG40	DDR0_DQ_127/DDR0_DQ_127	DDR0_CK0_127	AW18	M_A_CLK1
(11) M_A_DQ128	AE38	DDR0_DQ_128/DDR0_DQ_128	DDR0_CK0_128	AW18	M_A_CLK1
(11) M_A_DQ129	AE37	DDR0_DQ_129/DDR0_DQ_129	DDR0_CK0_129	AW18	M_A_CLK1
(11) M_A_DQ130	AG38	DDR0_DQ_130/DDR0_DQ_130	DDR0_CK0_130	AW17	M_A_CLK1
(11) M_A_DQ131	AG37	DDR0_DQ_131/DDR0_DQ_131	DDR0_CK0_131	AW17	M_A_CLK1
(11) M_A_DQ132	AE39	DDR0_DQ_132/DDR0_DQ_132	DDR0_CK0_132	AW18	M_A_CLK1
(11) M_A_DQ133	AE40	DDR0_DQ_133/DDR0_DQ_133	DDR0_CK0_133	AW18	M_A_CLK1
(11) M_A_DQ134	AG39	DDR0_DQ_134/DDR0_DQ_134	DDR0_CK0_134	AW18	M_A_CLK1
(11) M_A_DQ135	AG40	DDR0_DQ_135/DDR0_DQ_135	DDR0_CK0_135	AW18	M_A_CLK1
(11) M_A_DQ136	AE38	DDR0_DQ_136/DDR0_DQ_136	DDR0_CK0_136	AW18	M_A_CLK1
(11) M_A_DQ137	AE37	DDR0_DQ_137/DDR0_DQ_137	DDR0_CK0_137	AW18	M_A_CLK1
(11) M_A_DQ138	AG38	DDR0_DQ_138/DDR0_DQ_138	DDR0_CK0_138	AW17	M_A_CLK1
(11) M_A_DQ139	AG37	DDR0_DQ_139/DDR0_DQ_139	DDR0_CK0_139	AW17	M_A_CLK1
(11) M_A_DQ140	AE39	DDR0_DQ_140/DDR0_DQ_140	DDR0_CK0_140	AW18	M_A_CLK1
(11) M_A_DQ141	AE40	DDR0_DQ_141/DDR0_DQ_141	DDR0_CK0_141	AW18	M_A_CLK1
(11) M_A_DQ142	AG39	DDR0_DQ_142/DDR0_DQ_142	DDR0_CK0_142	AW18	M_A_CLK1
(11) M_A_DQ143	AG40	DDR0_DQ_143/DDR0_DQ_143	DDR0_CK0_143	AW18	M_A_CLK1
(11) M_A_DQ144	AE38	DDR0_DQ_144/DDR0_DQ_144	DDR0_CK0_144	AW18	M_A_CLK1
(11) M_A_DQ145	AE37	DDR0_DQ_145/DDR0_DQ_145	DDR0_CK0_145	AW18	M_A_CLK1
(11) M_A_DQ146	AG38	DDR0_DQ_146/DDR0_DQ_146	DDR0_CK0_146	AW17	M_A_CLK1
(11) M_A_DQ147	AG37	DDR0_DQ_147/DDR0_DQ_147	DDR0_CK0_147	AW17	M_A_CLK1
(11) M_A_DQ148	AE39	DDR0_DQ_148/DDR0_DQ_148	DDR0_CK0_148	AW18	M_A_CLK1
(11) M_A_DQ149	AE40	DDR0_DQ_149/DDR0_DQ_149	DDR0_CK0_149	AW18	M_A_CLK1
(11) M_A_DQ150	AG39	DDR0_DQ_150/DDR0_DQ_150	DDR0_CK0_150	AW18	M_A_CLK1
(11) M_A_DQ151	AG40	DDR0_DQ_151/DDR0_DQ_151	DDR0_CK0_151	AW18	M_A_CLK1
(11) M_A_DQ152	AE38	DDR0_DQ_152/DDR0_DQ_152	DDR0_CK0_152	AW18	M_A_CLK1
(11) M_A_DQ153	AE37	DDR0_DQ_153/DDR0_DQ_153	DDR0_CK0_153	AW18	M_A_CLK1
(11) M_A_DQ154	AG38	DDR0_DQ_154/DDR0_DQ_154	DDR0_CK0_154	AW17	M_A_CLK1
(11) M_A_DQ155	AG37	DDR0_DQ_155/DDR0_DQ_155	DDR0_CK0_155	AW17	M_A_CLK1
(11) M_A_DQ156	AE39	DDR0_DQ_156/DDR0_DQ_156	DDR0_CK0_156	AW18	M_A_CLK1
(11) M_A_DQ157	AE40	DDR0_DQ_157/DDR0_DQ_157	DDR0_CK0_157	AW18	M_A_CLK1
(11) M_A_DQ158	AG39	DDR0_DQ_158/DDR0_DQ_158	DDR0_CK0_158	AW18	M_A_CLK1

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170828 Leon:Change CPU1 to 062.10015.0081 for SB
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HDMI OUT

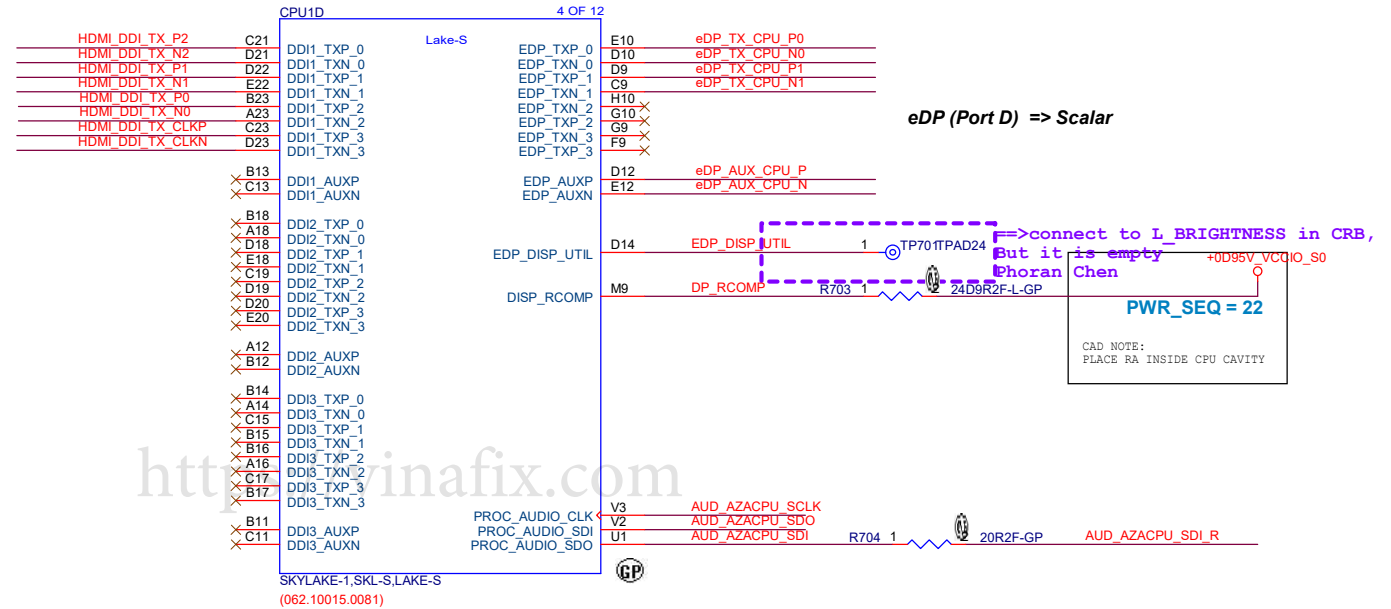
[56] HDMI_DDI_TX_P2 <<—
[56] HDMI_DDI_TX_N2 <<—
[56] HDMI_DDI_TX_P1 <<—
[56] HDMI_DDI_TX_N1 <<—
[56] HDMI_DDI_TX_P0 <<—
[56] HDMI_DDI_TX_N0 <<—
[56] HDMI_DDI_TX_CLKP <<—
[56] HDMI_DDI_TX_CLKN <<—

EDP

[95] eDP_TX_CPU_P0 <<—
[95] eDP_TX_CPU_N0 <<—
[95] eDP_TX_CPU_P1 <<—
[95] eDP_TX_CPU_N1 <<—
[95] eDP_AUX_CPU_P <<—
[95] eDP_AUX_CPU_N <<—

[20] AUD_AZACPU_SDO >>—
[20] AUD_AZACPU_SDI_R <<—
[20] AUD_AZACPU_SCLK >>—

170828 Leon:Change CPU1 to 062.10015.0081 for SB



wistron®

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
007_CPU_(DDI/EDP)

Size
B

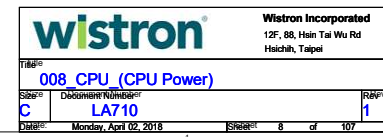
Document Number
LA710

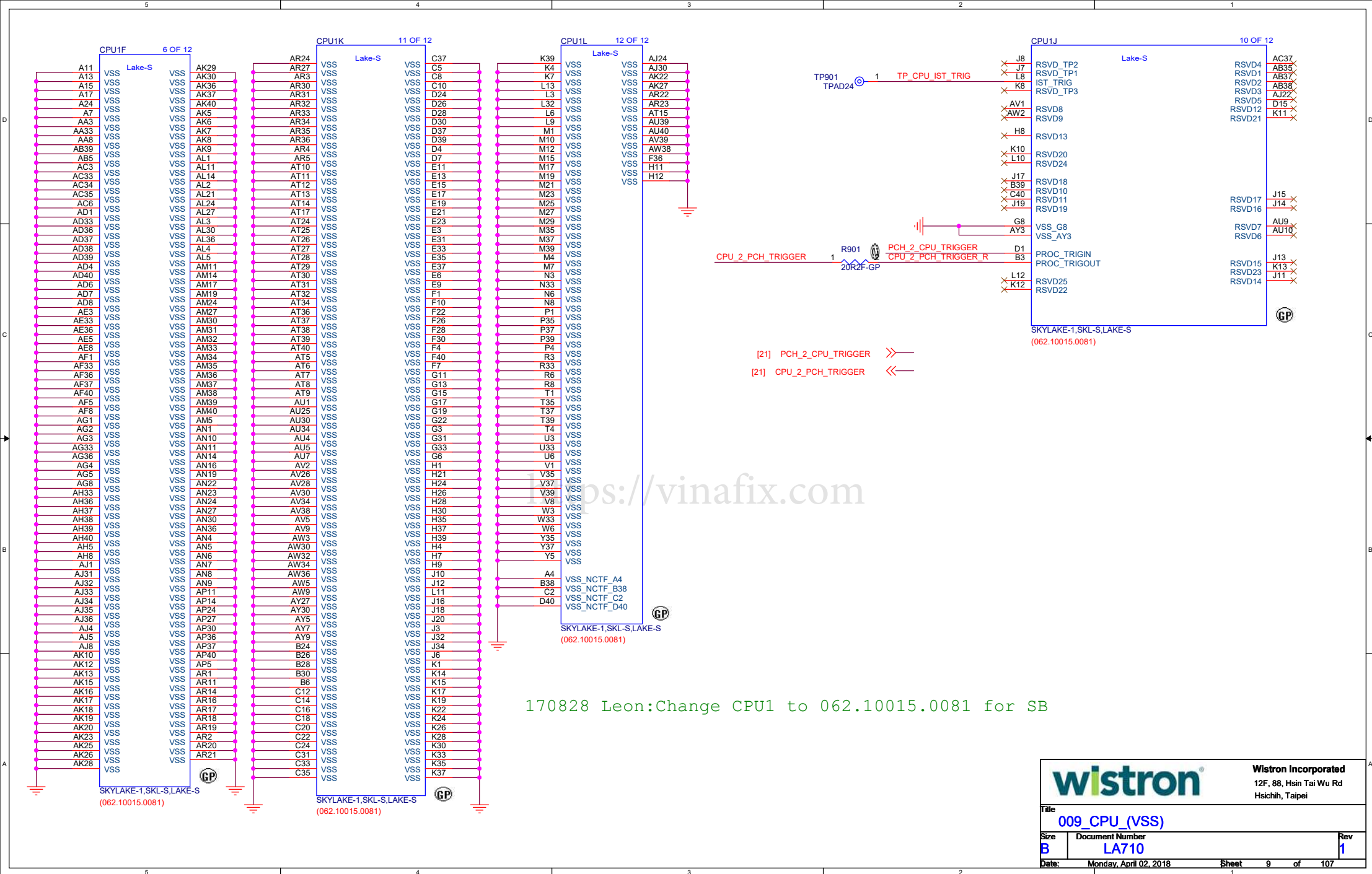
Date: Monday, April 02, 2018

Sheet 7 of 107

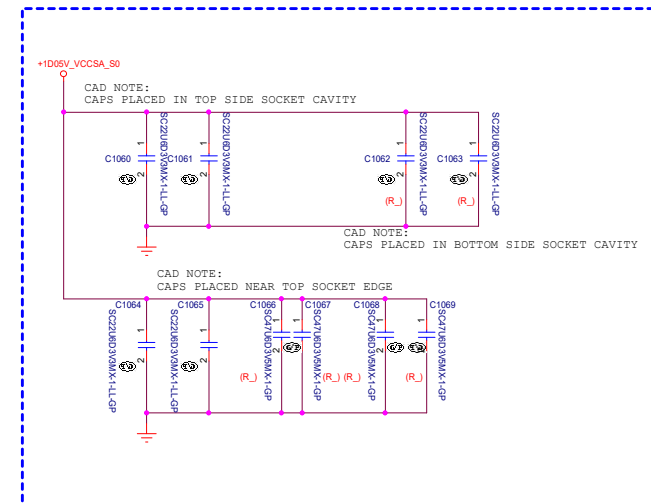
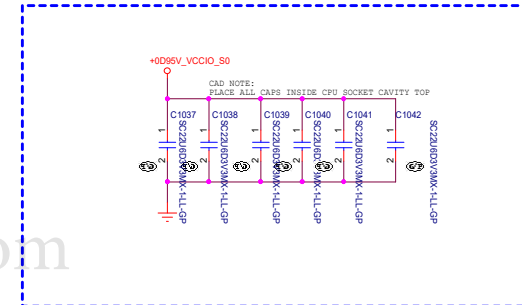
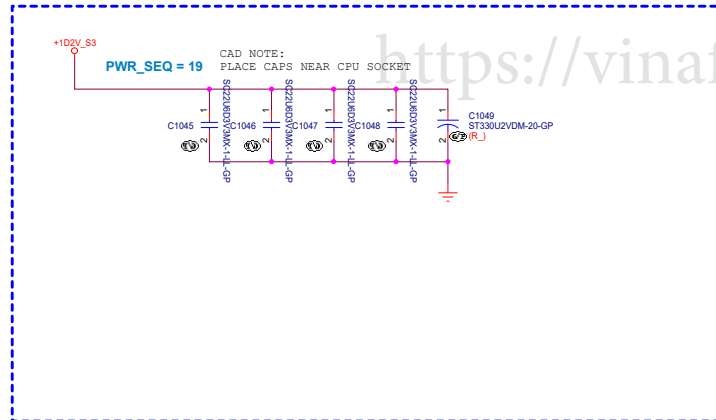
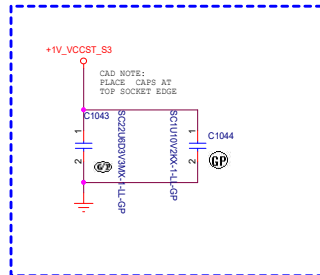
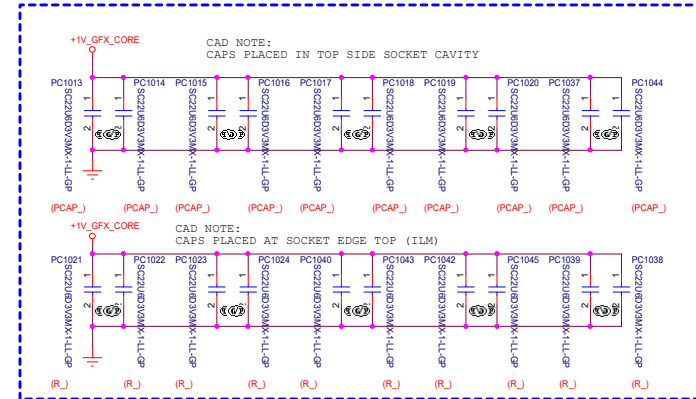
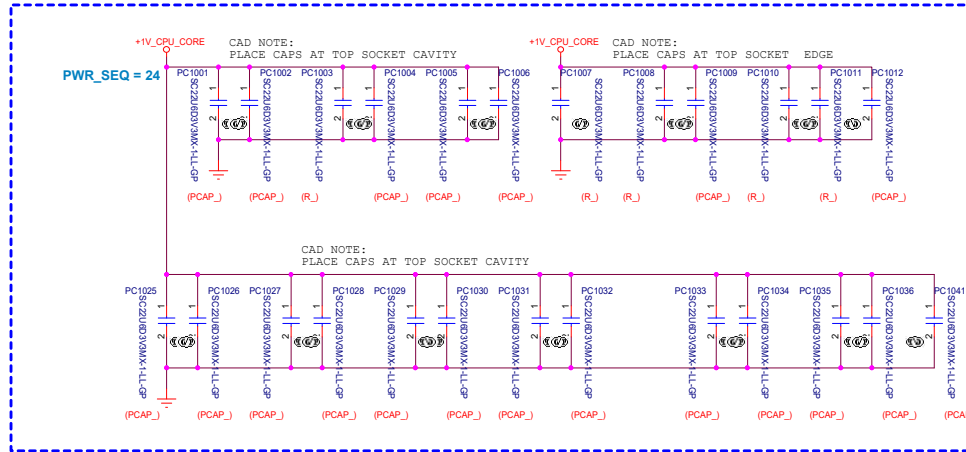
Rev
1

[46]	VCCCORE_SENSE	⏏
[46]	VSSCORE_SENSE	⏏
[46]	VCCGT_SENSE	⏏
[46]	VSSGT_SENSE	⏏
[50]	VCCSA_SENSE	⏏
[50]	VCCIO_SENSE	⏏
[50]	VCCSA_VSS_SEN	⏏
[50]	VCCIO_VSS_SEN	⏏
[20,24,35,36,40]	SLP_S4_N	⏏

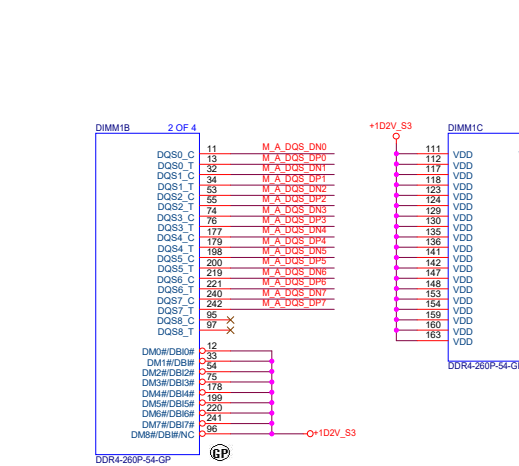




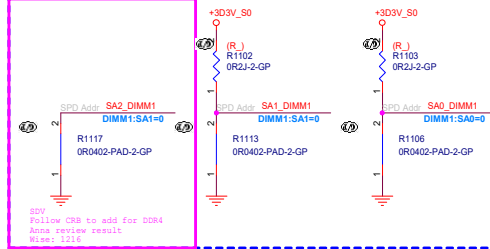
EE Leon: VCORE / GT cap from power team request



CHANNEL-A XMM1, A0, H=8mm

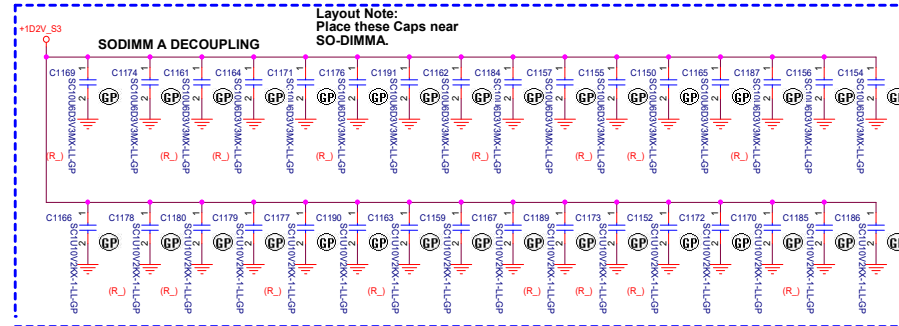


SPD Address of DIMM1

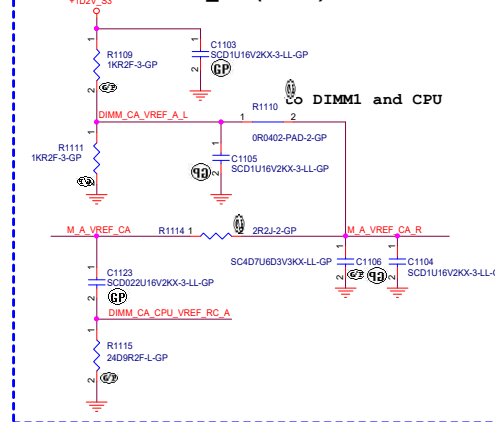


SPD SA2	0
SPD SA1	0
SPD SA0	0

Note:
SA0 DIMM1 = 0, SA1 DIMM1 = 0
SO-DIMMA SPD Address is 0x0A
SO-DIMMA TS Address is 0x30



VREF_CA (Ch. A)




SPD Address Table

Device	SMBus_0 8-bit Address(hex)
DIMM A0	Write Addr: 0xA0 Read Addr: 0xA1 SA1=0, SA0=0
DIMM A1	Write Addr: 0xA2 SA1=0, SA0=1
DIMM B0	Write Addr: 0xA4 SA1=1, SA0=0
DIMM B1	Write Addr: 0xA5 SA1=1, SA0=1
1 0 1 1 0 0 SA1 SA0 0	

Note: 0' 3~7 bit as default

	5	4	3	2	1
D					D
C					C
B					B
A					A
	5	4	3	2	1

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Wistron Incorporated
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Title

012_DDR DIMM_2

Size

Document Number

Rev

A

LA710

1

Date:

Monday, April 02, 2018

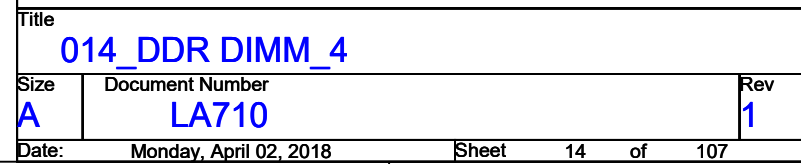
Sheet

12

of

107

A



SPI0

[09] SPI0_SI_XDP
[22,25,91] SPI0_SI_ROM
[22,25,91] SPI0_SO_ROM
[25] SPI0_CS0_ROM_N
[25,91] SPI0_CLK_ROM

TPM

[24,62] PLTRST_N
[22] GPP_H_12
[22] LPS5_GSPH0_MOSI
[22] LPS5_GSPH0_MOSI
[65] BRIGHTNESS_PLUS
[65] BRIGHTNESS_MINUS
[91] SPI0_CS_TPM

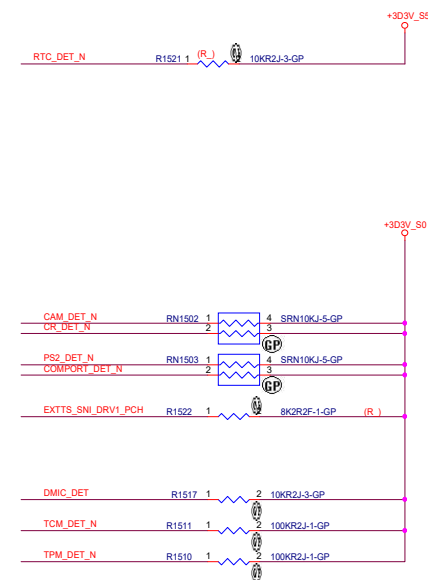
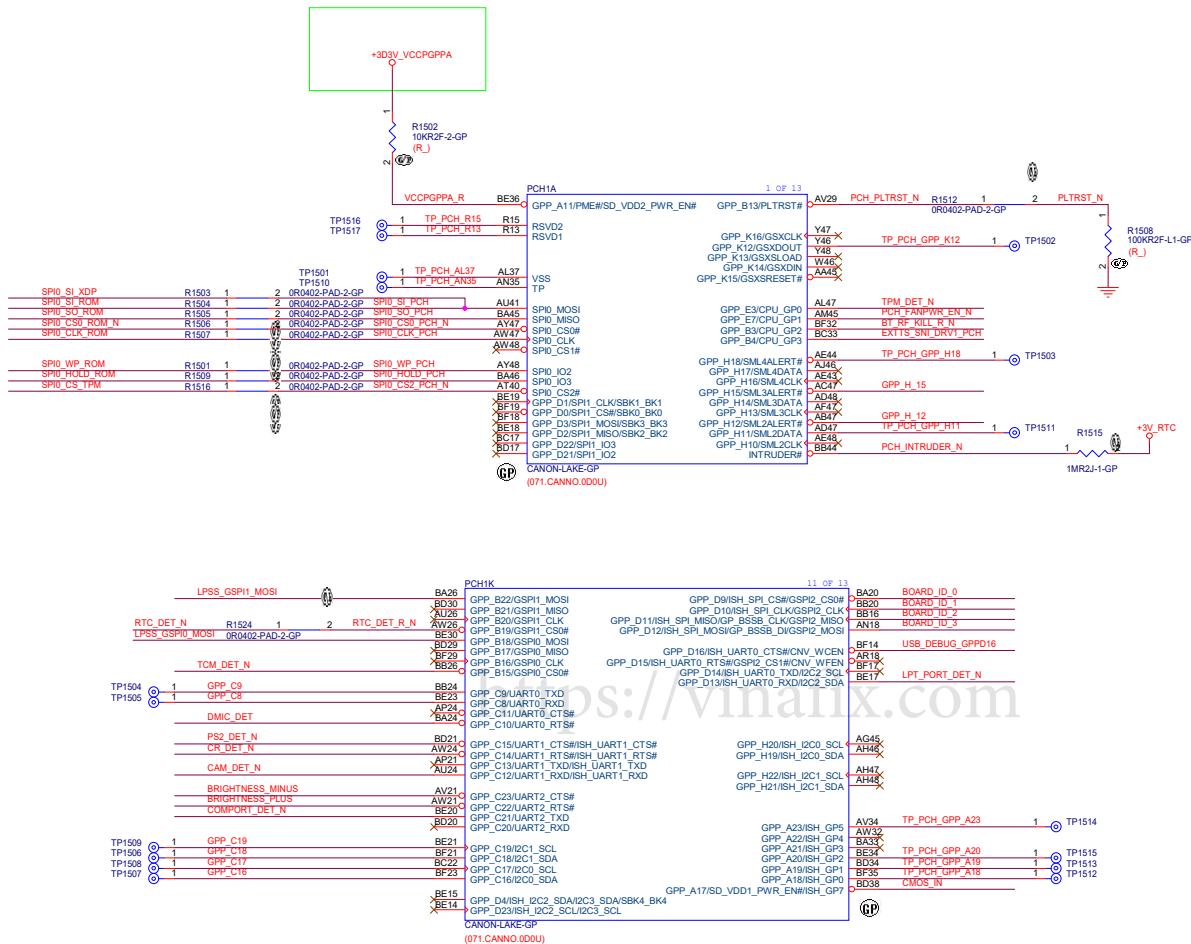
[39] PCH_FANPWR_EN_N
[61] BT_RF_KILL_R_N

[65] DMIC_DET
[24,25] RTC_DET_N
[91] TCM_DET_N
[91] TPM_DET_N
[65] CAM_DET_N
[33] CR_DET_N

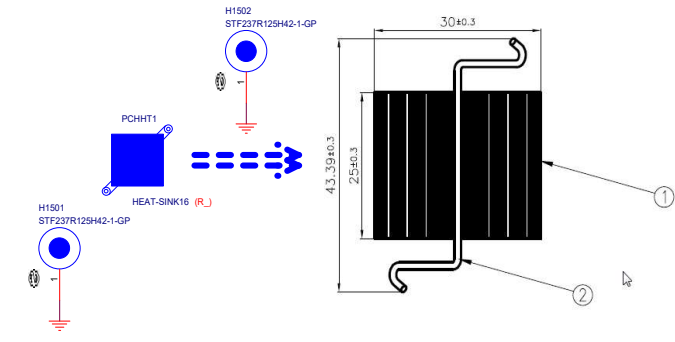
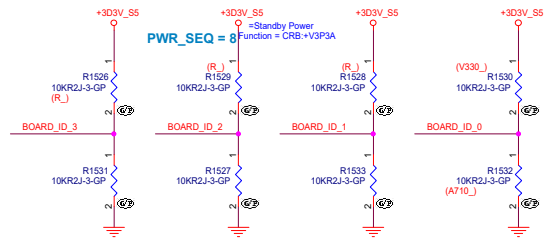
[65] PS2_DET_N
[92] COMPORT_DET_N
[92] LPT_PORT_DET_N
[25] CMOS_IN

USB DEBUG GPIO

[38] USB_DEBUG_GPPD16



BOARD ID



[B1] CLINK_CLK_PCH
[B1] CLINK_DATA_PCH
[B1] CLINK_RST_PCH_N

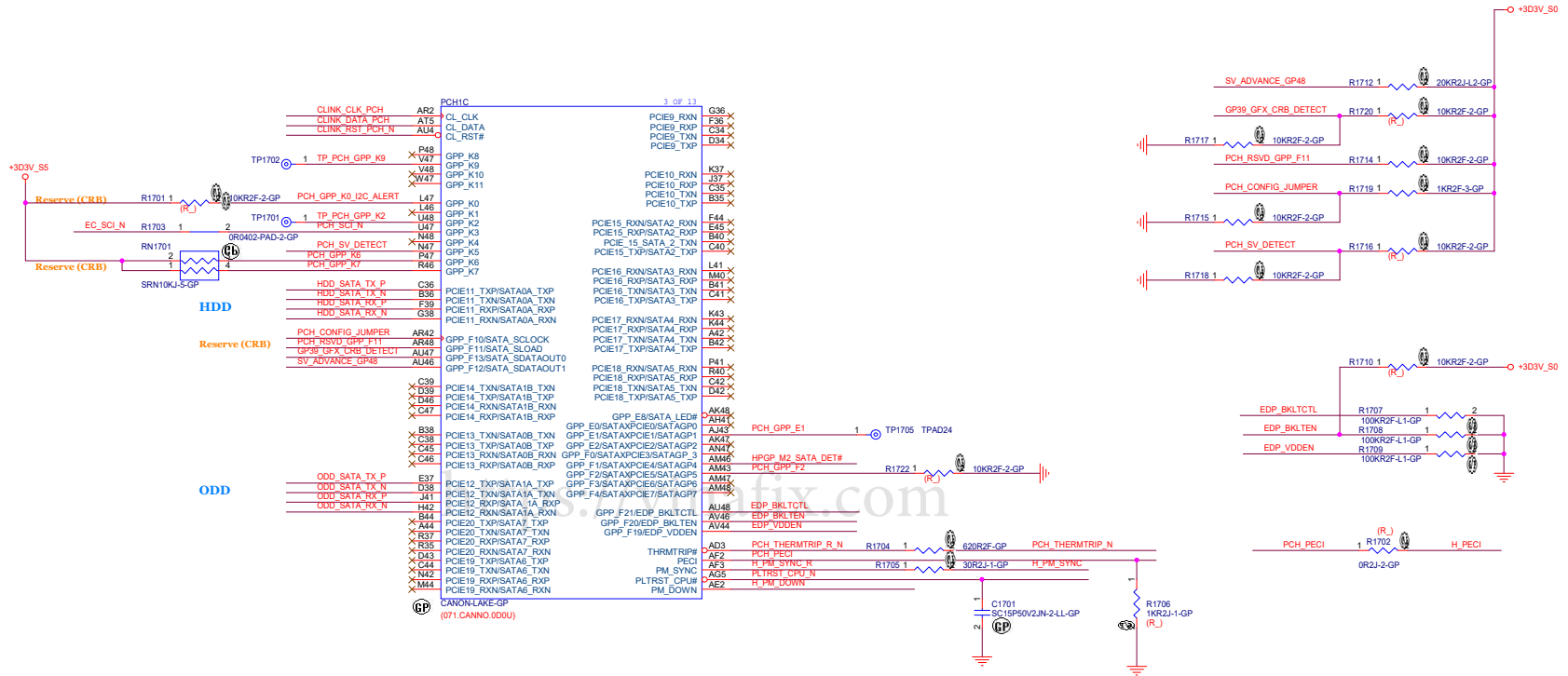
HDD
[60] HDD_SATA_TX_P
[60] HDD_SATA_TX_N
[60] HDD_SATA_RX_P
[60] HDD_SATA_RX_N

ODD
[60] ODD_SATA_TX_P
[60] ODD_SATA_TX_N
[60] ODD_SATA_RX_P
[60] ODD_SATA_RX_N

[B2] HPGP_M2_SATA_DET#
[24] EC_SCI_N
[4] PCH_THERMTRIP_N

[4,24] H_PECI
[4] H_PM_SYNC
[4] PLTRST_CPU_N
[4] H_PM_DOWN

[24,55] EDP_BKLTEN
[95] EDP_BKLTCTL



USB3.0

[36] USB1_USB30_TX_N
[36] USB1_USB30_TX_P
[36] USB1_USB30_RX_N
[36] USB1_USB30_RX_P

[36] USB2_USB30_TX_N
[36] USB2_USB30_TX_P
[36] USB2_USB30_RX_N
[36] USB2_USB30_RX_P

[36] USB3_USB30_TX_P
[36] USB3_USB30_TX_N
[36] USB3_USB30_RX_P
[36] USB3_USB30_RX_N

[35] USB4_USB30_TX_P
[35] USB4_USB30_TX_N
[35] USB4_USB30_RX_P
[35] USB4_USB30_RX_N

[36] USB5_USB30_TX_N
[36] USB5_USB30_TX_P
[36] USB5_USB30_RX_N
[36] USB5_USB30_RX_P

[34] CHARGER_USB30_TX_N
[34] CHARGER_USB30_TX_P
[34] CHARGER_USB30_RX_N
[34] CHARGER_USB30_RX_P

171114 EE Leon: SWAP USB3 Port 1 & 2 for layout request

Rear USB 3.1 / Gen2 / Port2

Rear USB 3.1 / Gen2 / Port1

Front USB 3.0 / Gen1 / Port6
Support USB charger

Rear USB 3.0 / Gen1 / Port5
Support USB power on

Rear USB 3.1 / Gen2 / Port3

Front USB 3.1 / Gen2 / Port4
Support USB Debug

USB2_USB30_TX_N	F9	USB31_1_TXN	GPP_A1/LAD0/ESPI_IO0
USB2_USB30_TX_P	F7	USB31_1_TXP	GPP_A2/LAD1/ESPI_IO1
USB2_USB30_RX_N	D11	USB31_1_RXN	GPP_A3/LAD2/ESPI_IO2
USB2_USB30_RX_P	C11	USB31_1_RXP	GPP_A4/LAD3/ESPI_IO3
USB1_USB30_TX_N	C3	USB31_2_TXN	GPP_A5/LFRAME#/ESPI_CS0#
USB1_USB30_TX_P	D4	USB31_2_TXP	GPP_A6/SERIRQ/ESPI_CS1#
USB1_USB30_RX_N	B9	USB31_2_RXN	GPP_A7/PIRQA#/ESPI_ALERT0#
USB1_USB30_RX_P	C9	USB31_2_RXP	GPP_A0/RCIN#/ESPI_ALERT1#
CHARGER_USB30_TX_N	C17	USB31_6_TXN	GPP_A9/CLKOUT_LPC0/ESPI_CLK
CHARGER_USB30_TX_P	C16	USB31_6_TXP	GPP_A10/CLKOUT_LPC1
CHARGER_USB30_RX_N	G14	USB31_6_RXN	GPP_K19/SMI#
CHARGER_USB30_RX_P	F14	USB31_6_RXP	GPP_K18/NMI#
USB5_USB30_TX_N	C15	USB31_5_TXN	GPP_E6/SATA_DEVSLP2
USB5_USB30_TX_P	B15	USB31_5_TXP	GPP_E5/SATA_DEVSLP1
USB5_USB30_RX_N	J13	USB31_5_RXN	GPP_F4/SATA_DEVSLP0
USB5_USB30_RX_P	K13	USB31_5_RXP	GPP_F9/SATA_DEVSLP7
USB3_USB30_TX_P	G12	USB31_3_TXP	GPP_F8/SATA_DEVSLP6
USB3_USB30_TX_N	F11	USB31_3_TXN	GPP_F7/SATA_DEVSLP5
USB3_USB30_RX_P	C10	USB31_3_RXP	GPP_F6/SATA_DEVSLP4
USB3_USB30_RX_N	B10	USB31_3_RXN	GPP_F5/SATA_DEVSLP3
USB4_USB30_TX_P	C14	USB31_4_TXP	
USB4_USB30_TX_N	B14	USB31_4_TXN	
USB4_USB30_RX_P	J15	USB31_4_RXP	
USB4_USB30_RX_N	K16	USB31_4_RXN	

PCH1F

6 OF 13

CANON-LAKE-GP
(071.CANNO.0D0U)

LPC interface

[24,68,91] LPC_AD_SIO_P0
[24,68,91] LPC_AD_SIO_P1
[24,68,91] LPC_AD_SIO_P2
[24,68,91] LPC_AD_SIO_P3

[24,68,91] LPC_FRAME#_SIO
[24,91] SER_IRQ
[19,68,91] LPC_CLK1_PCH24M_TPM

[24] EC_KBRST_N

[24] LPC_CLK0_PCH24M_SIO

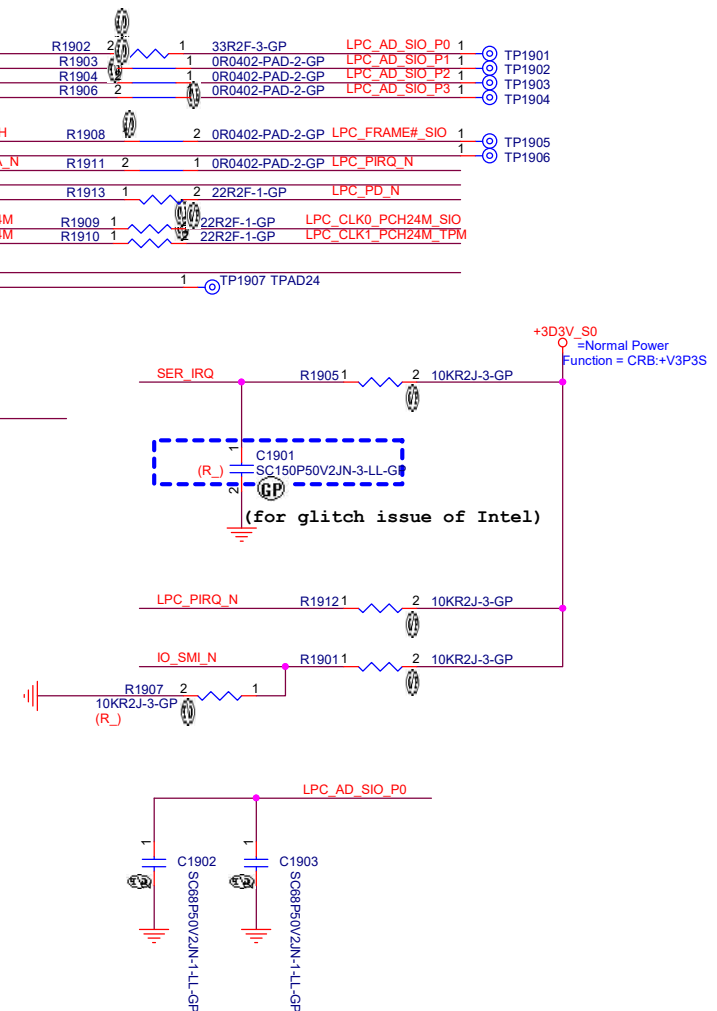
[91] LPC_PD_N
[24] LPC_PIRQ_N

[62] PCH_DEVSLP_N

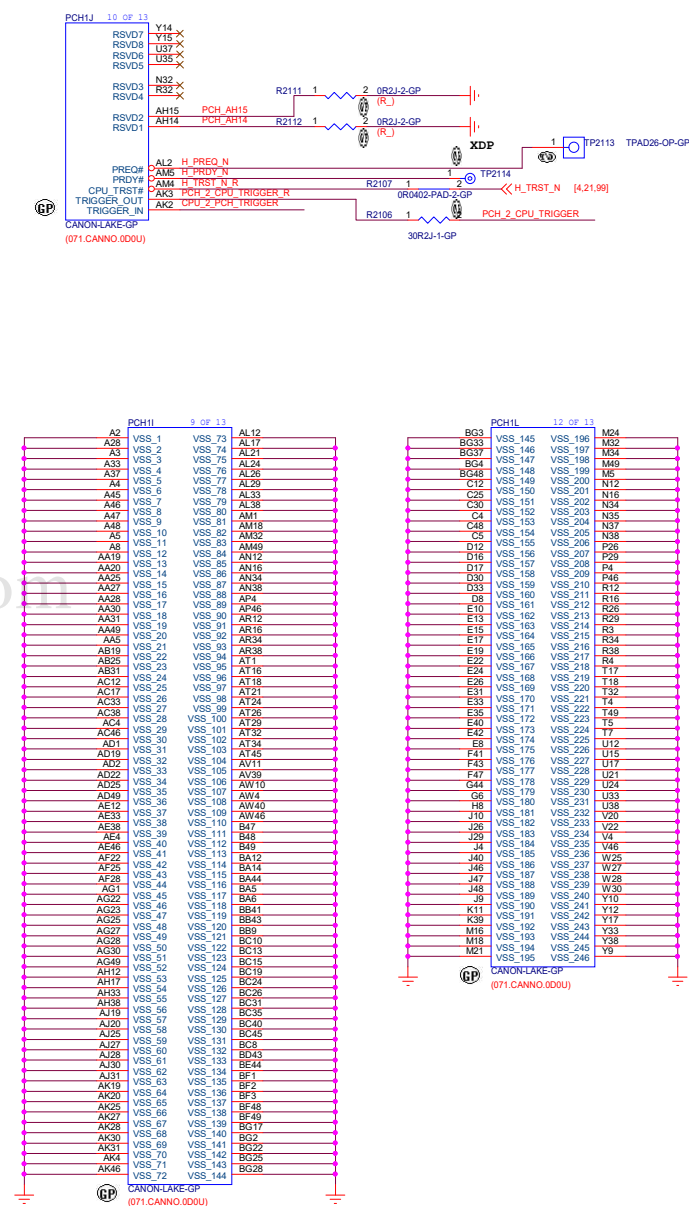
DEBUG Card

[19,68,91] LPC_CLK1_PCH24M_TPM

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wistron		Wistron Incorporated	
12F, 88, Hsin Tai Wu Rd		Hsieh, Taipei	
Title			
019_PCH_(USB/ESPI)			
Size	Document/Number		Rev
B	LA710		1
Date:	Monday, April 02, 2018		Sheet 19 of 107



PCH STRAP FUNCTIONS

SPI MOSI (SPI0_MOSI)	EDS: Reserved External pull-up is required. Recommend 100K if pulled up to 3.3V Rising edge of RSMRST#
SPI MISO (SPI0_MISO)	0: Disable JTAG ODT 1: Enable JTAG ODT The internal PU resistor is enabled when RSMRST# is asserted
SPI IO2 (SPI0_IO2)	EDS: Reserved External pull-up is required. Recommend 100K if pulled up to 3.3V Rising edge of RSMRST#
SPI IO3 (SPI0_IO3)	EDS: Reserved External pull-up is required. Recommend 100K if pulled up to 3.3V Rising edge of RSMRST#

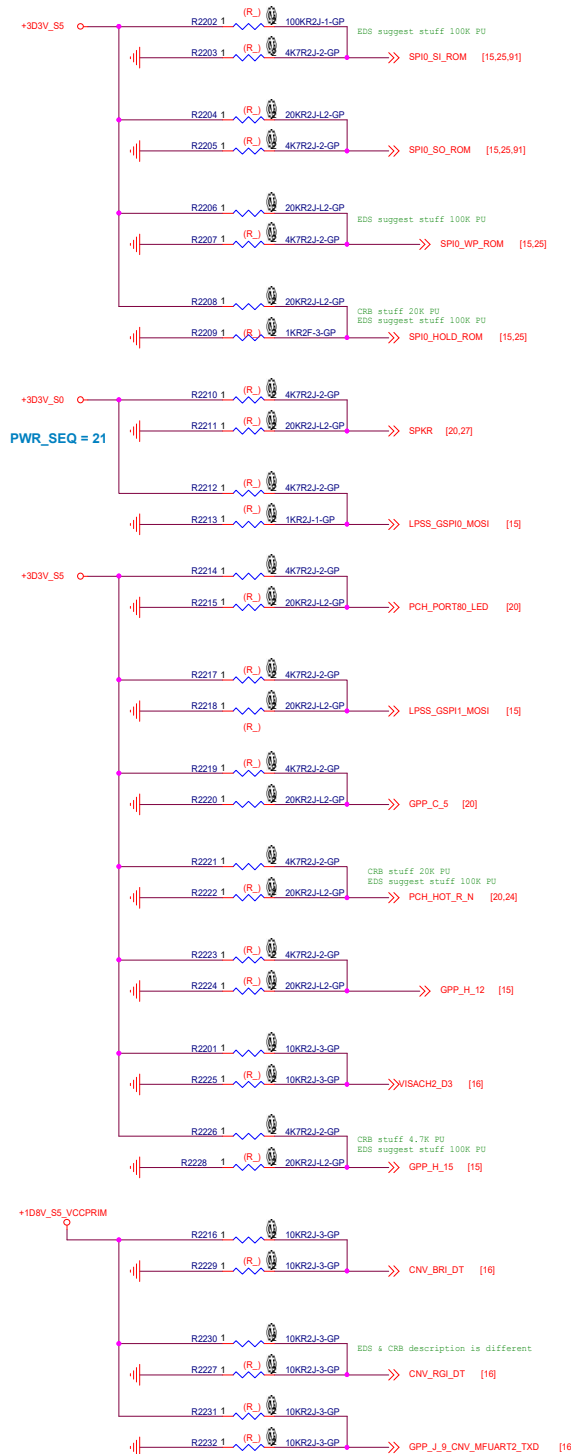
SPKR (SPKR / GPP_B14)	0: Disable Top Swap mode. (Default) 1: Enable Top Swap mode. PCH internal pull-down is disabled after PCH_PWROK deasserts.
LPSS GSPI0 MOSI (GPP_B18/GSPI0_MOSI)	0: Disable No Reboot mode. (Default) 1: Enable No Reboot mode This function is useful when running ITP/XDP. PCH internal pull-down is disabled after PCH_PWROK deasserts.
PCH_PORT80_LED (GPP_C2/SMBALERT#)	0: Disable TSL confidentiality 1: Enable TSL confidentiality (default) PCH HAS INTERNAL WEAK PD Rising edge of RSMRST#
LPSS GSPI1 MOSI (GPP_B22/GSPI1_MOSI)	BOOT SELECT STRAP 0: SPI select (Default) 1: LPC select PCH HAS INTERNAL WEAK PD Rising edge of PCH_PWROK
GPP C 5 (GPP_C5/SML0ALERT#)	ESPI/LPC SELECT STRAP 0: LPC is selected for EC. (Default) 1: eSPI is selected for EC. PCH HAS INTERNAL WEAK PD Rising edge of RSMRST#
PCH HOT R N (GPP_B23/SML1ALERT#/PCHHOT#)	0: Disable DCI OOB (Default) 1: Enable DCI OOB PCH HAS INTERNAL WEAK PD Rising edge of RSMRST#
GPP H 12 (GPP_H12/SML2ALERT#)	ESPI flash sharing mode 0: Master attached flash sharing (Default) 1: Slave attached flash sharing PCH has internal weak PD. Rising edge of RSMRST#
VISACH2_D3 (GPP_E12)	DFX test mode 0: XTAL input is single ended. 1: XTAL input is differential. The internal PD resistor is disabled after RSMRST# de-asserts
GPP H15 / SML3ALERT#	EDS: Reserved External pull-up is required. Recommend 100K if pulled up to 3.3V Rising edge of RSMRST#
GPP J4 / CNV_BRI_DT / UART0_RTS#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. Rising edge of RSMRST#

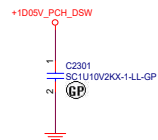
GPP J6 /
CNV_RGI_DT /
UART0_TXD

An external pull-up or pull-down is required.
0 = Integrated CNV1 enable.
1 = Integrated CNV1 disable.
Rising edge of RSMRST#

GPP J9

The signal has a weak internal pull-down
0 = VCCSPI is connected to 3.3V rail
1 = VCCSPI is connected to 1.8V rail
Rising edge of RSMRST#



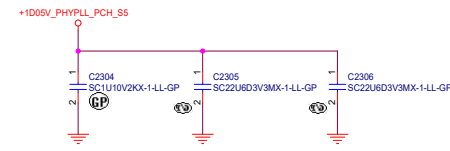


DESIGN NOTE:
BOARD CAP FOR +1P05V_PCH_DSW
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE

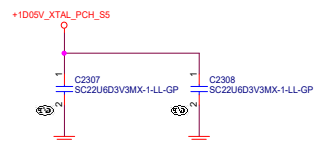


DESIGN NOTE:
BOARD CAP FOR +1V_PCH_S5
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE

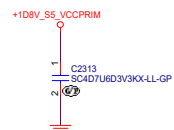
DESIGN NOTE:
BOARD CAP FOR +1V_PCH_S5
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE



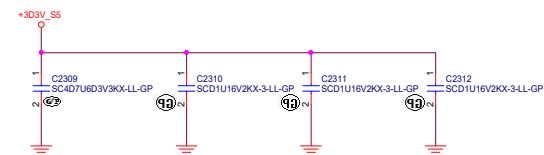
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE



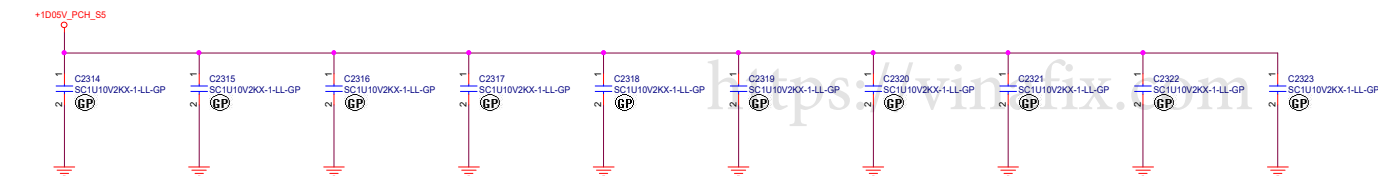
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE



DESIGN NOTE:
EDGE CAP FOR +1D8V_S5
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE

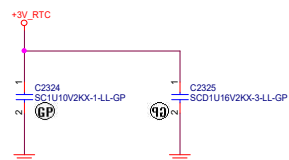


CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE

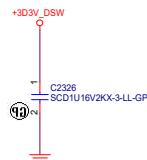


CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE

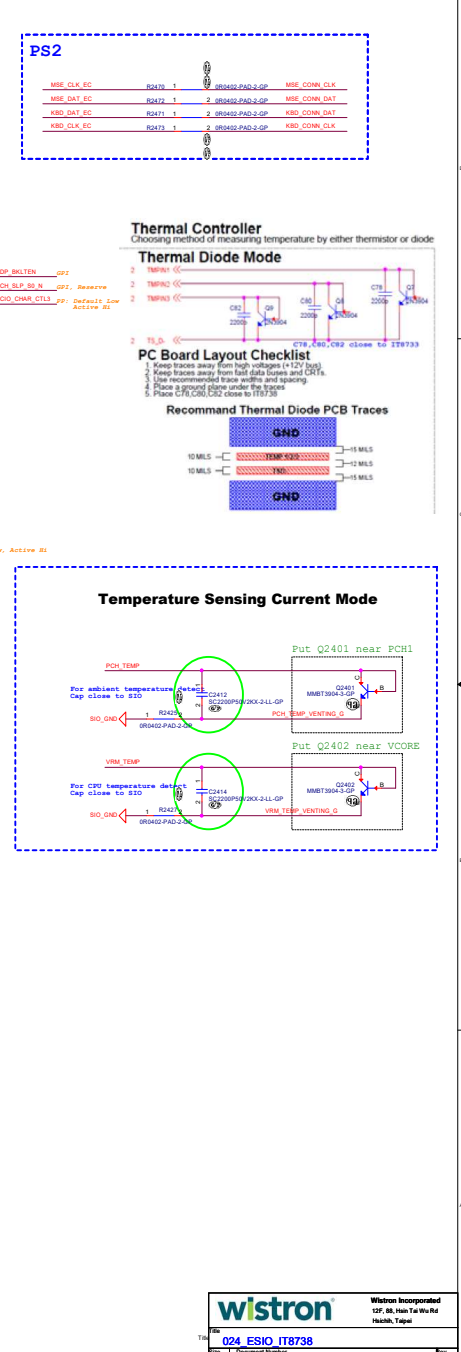
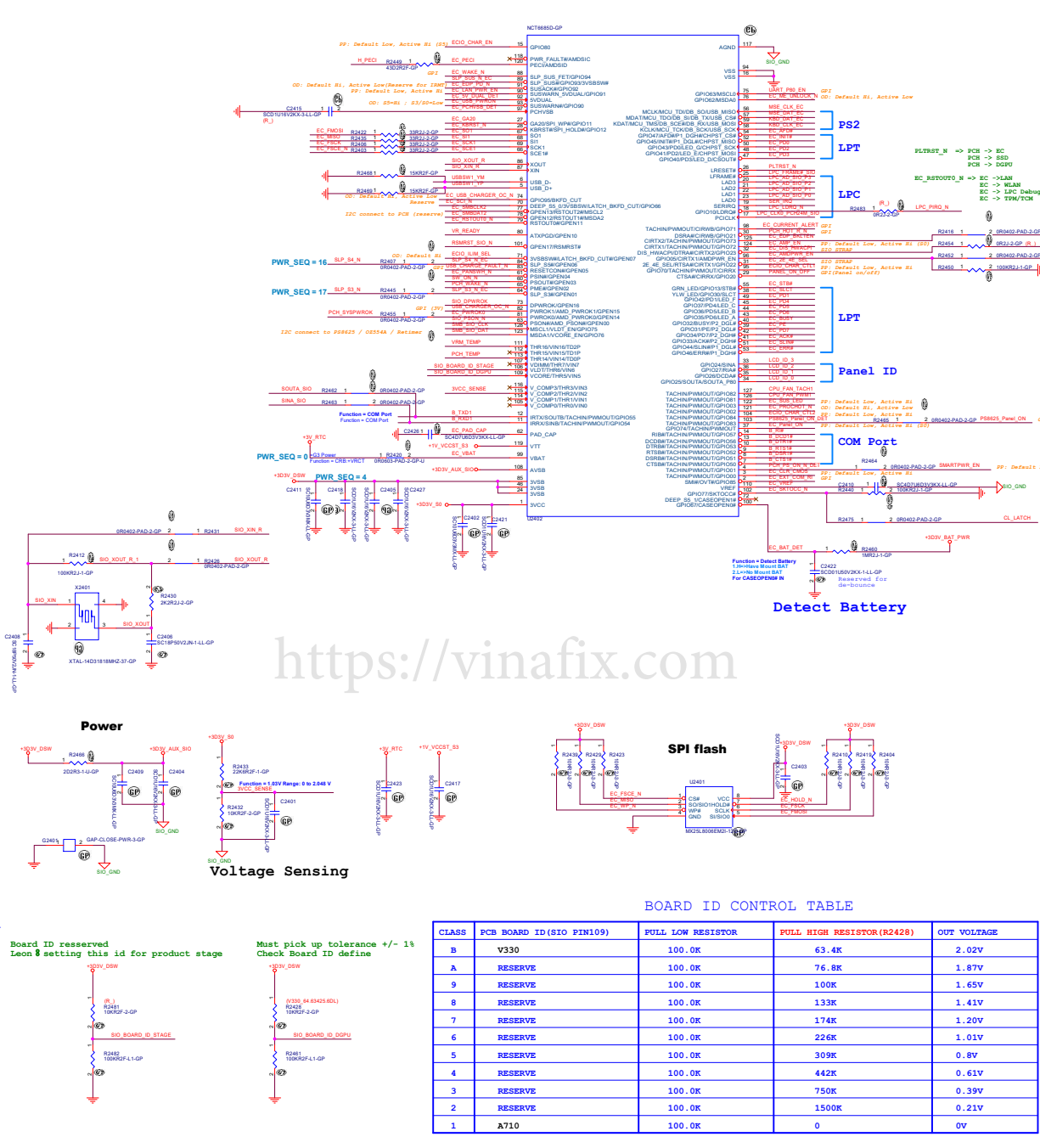
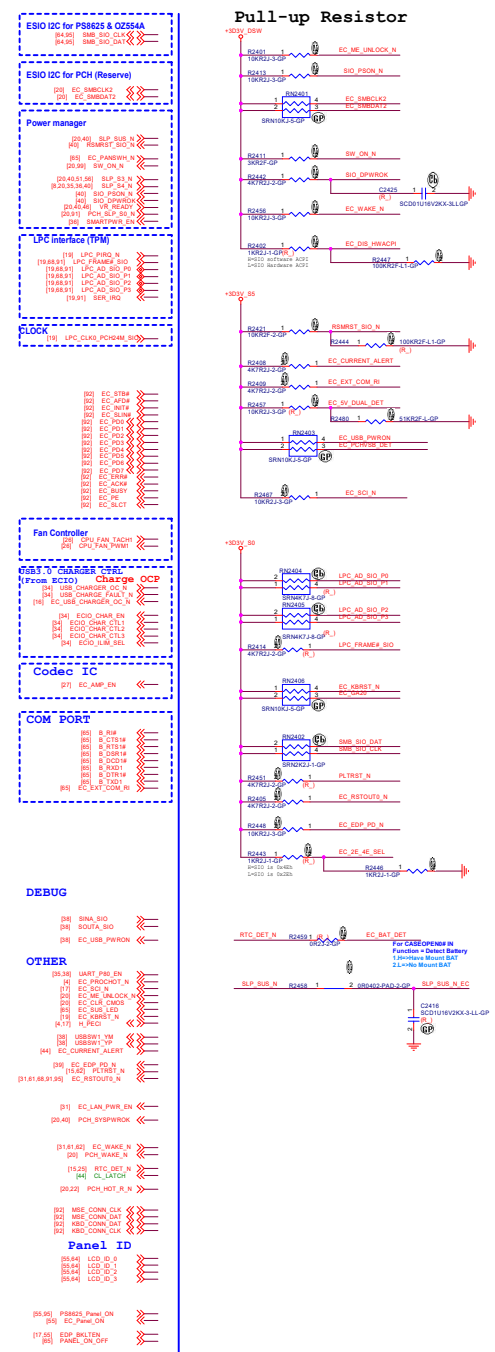
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE



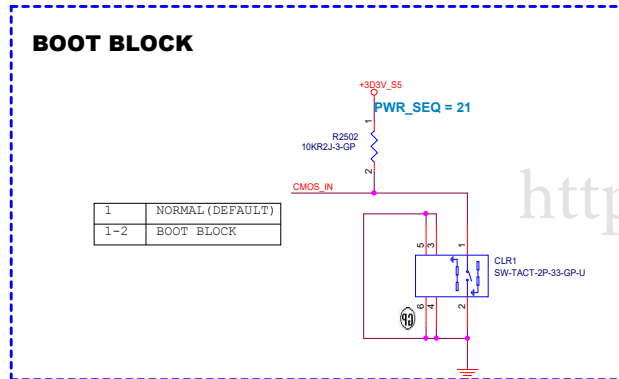
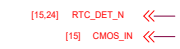
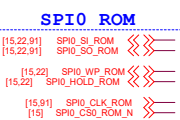
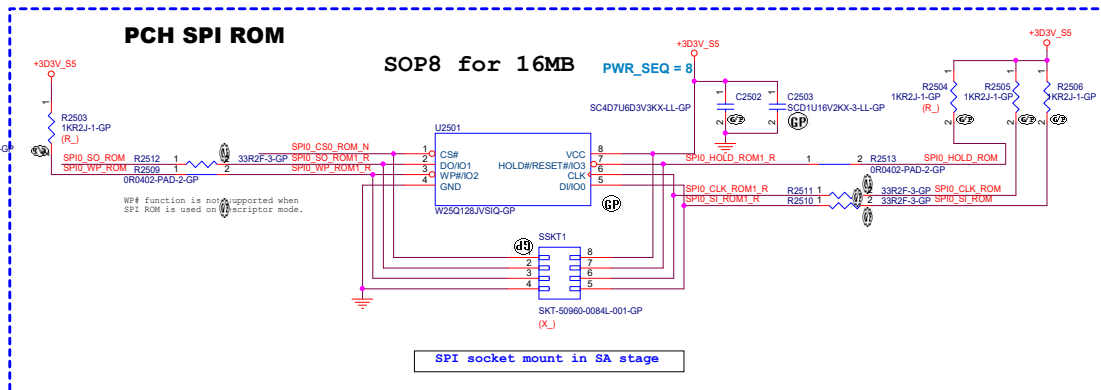
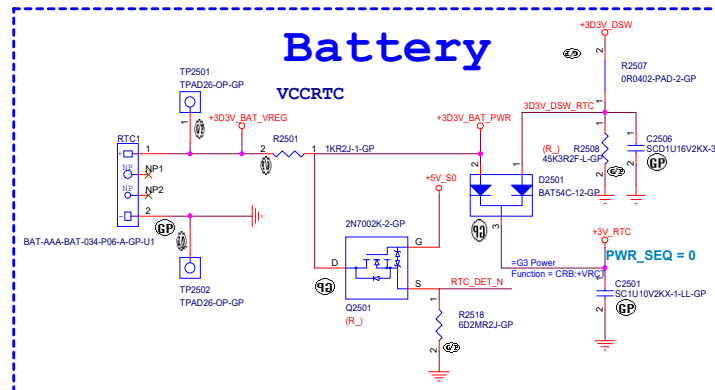
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE



CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE

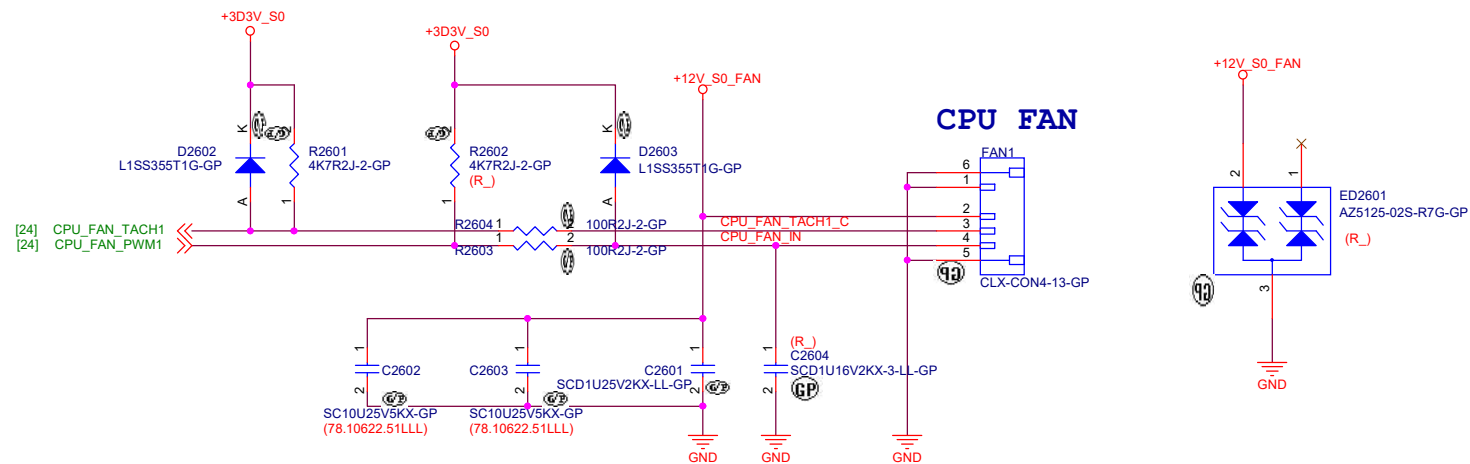


BOARD ID CONTROL TABLE				
CLASS	PCB BOARD ID(SIO PIN109)	FULL LOW RESISTOR	FULL HIGH RESISTOR(R2428)	OUT VOLTAGE
B	V330	100.0K	63.4K	2.02V
A	RESERVE	100.0K	76.8K	1.87V
9	RESERVE	100.0K	100K	1.65V
8	RESERVE	100.0K	133K	1.41V
7	RESERVE	100.0K	174K	1.20V
6	RESERVE	100.0K	226K	1.01V
5	RESERVE	100.0K	309K	0.8V
4	RESERVE	100.0K	442K	0.61V
3	RESERVE	100.0K	750K	0.39V
2	RESERVE	100.0K	1500K	0.21V
1	A710	100.0K	0	0V



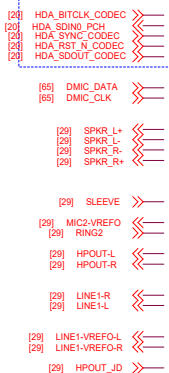
<https://vinafix.com>

SIO FAN CONTROL



<https://vinafix.com>

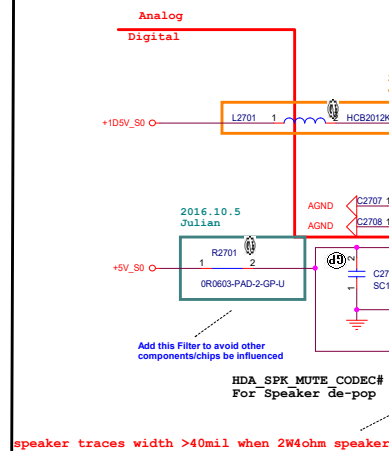
HD LINK



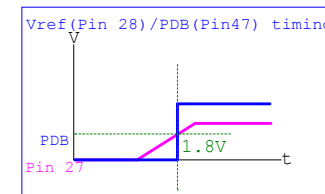
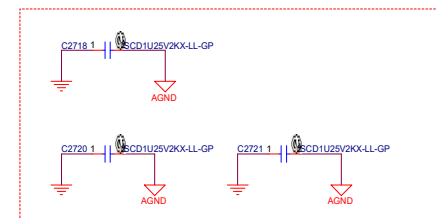
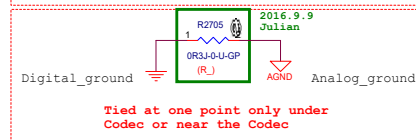
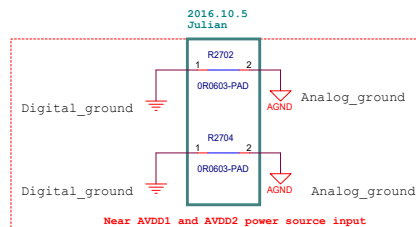
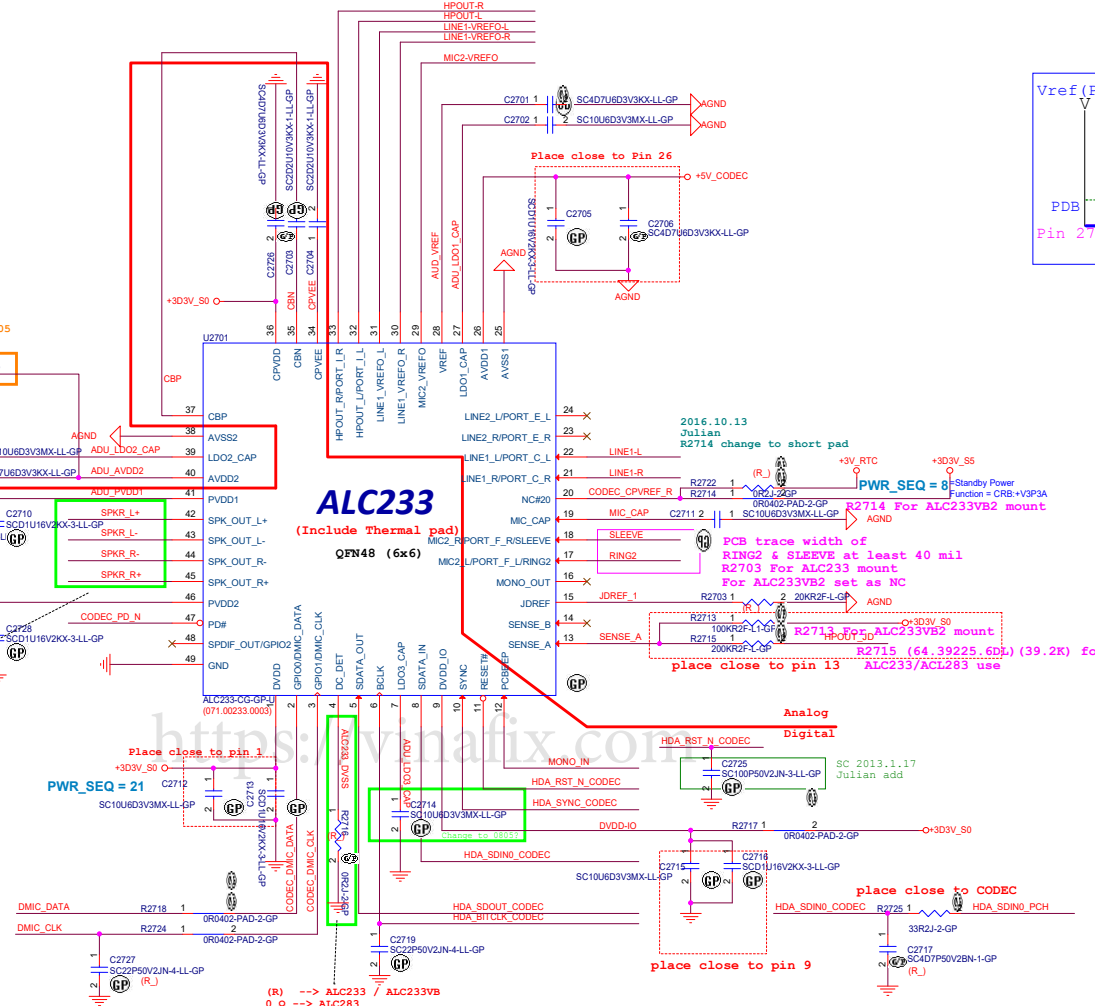
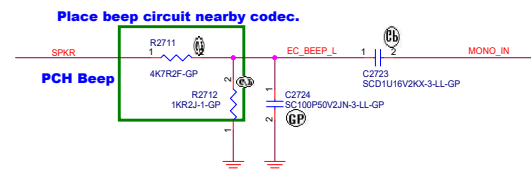
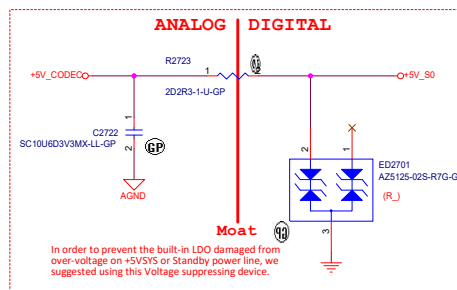
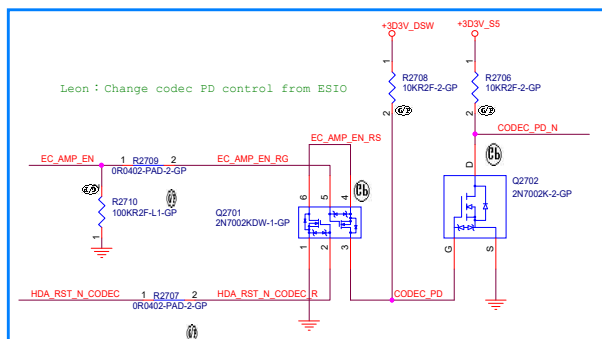
CODEC PD from ESIO



Buzzer from PCH



speaker traces width >40mil when 2W4ohm speaker



Reserved

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Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title

028_Audio DSP&_(R)

Size

A

Document Number

LA710

Rev

1

Date:

Monday, April 02, 2018

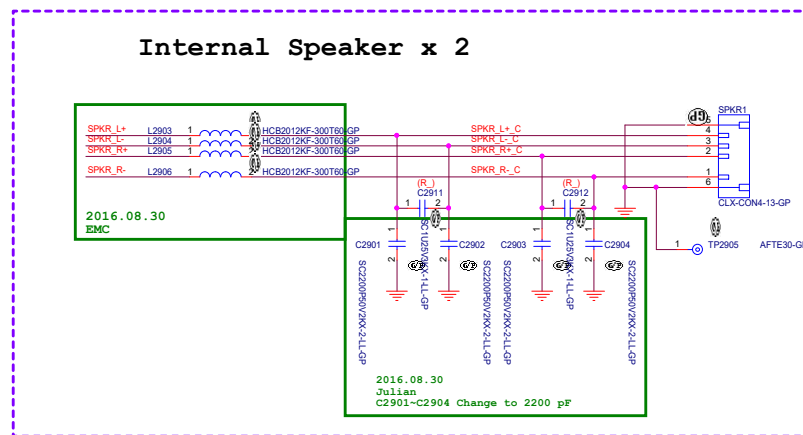
Sheet

28

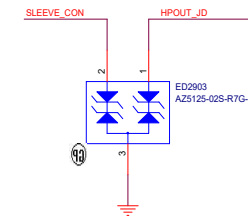
of

107

- [27] SPKR_L+ <<<
 [27] SPKR_L- <<<
 [27] SPKR_R- <<<
 [27] SPKR_R+ <<<
- [27] SLEEVE <<<
 [27] RING2 <<<
 [27] HPOUT-R <<<
 [27] HPOUT-L <<<
 [27] LINE1-R <<<
 [27] LINE1-L <<<
 [27] LINE1-VREFOL <<<
 [27] LINE1-VREFOR <<<
 [27] MIC2-VREFO <<<
 [27] HPOUT_ID <<<

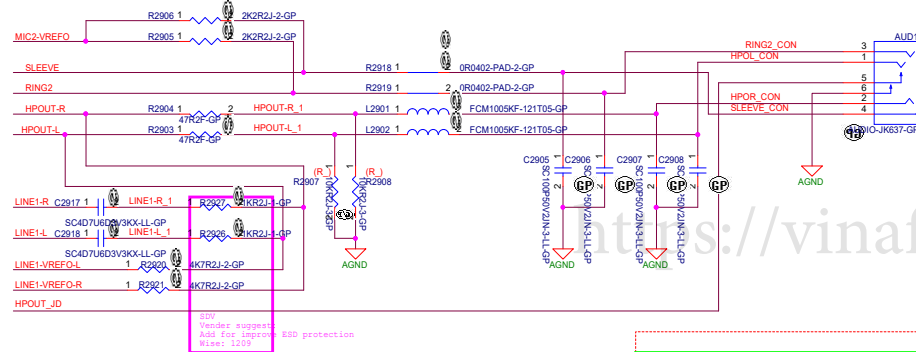


ESD



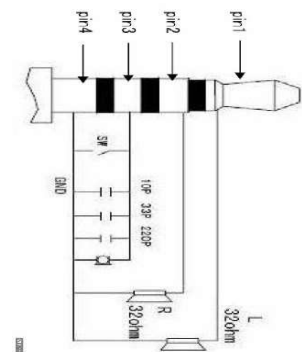
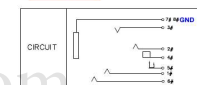
D2905 NEAR AUD1

UAJ Headset (ALC233 supported iPhone/Nokia headset, Headphone)



Pin Define:
 Pin1: Ring2
 Pin2: HP_L
 Pin3: HP_R
 Pin4: JD
 Pin5: AGND
 Pin6: Sleeve
 Pin7: GND
 Pin8: GND

B.COLOR
1.BLACK



4-pin 3.5mm Headset Connector Pinout

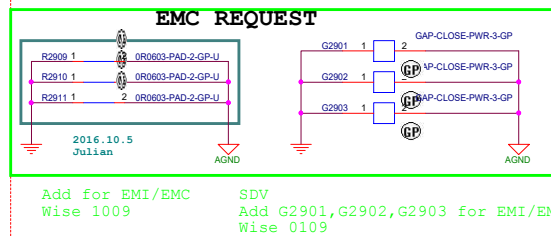


Nokia, Lenovo mobile

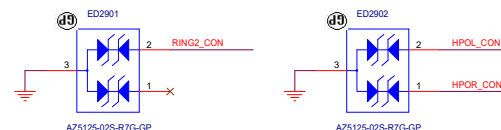
Pin Number	Pin Name	Description
1	Tip	Left Audio Out
2	Ring-1	Right Audio Out
3	Ring-2	Microphone
4	Sleeve	Ground / Common

iPhone, Samsung, Blackberry, HTC

Pin Number	Pin Name	Description
1	Tip	Left Audio Out
2	Ring-1	Right Audio Out
3	Ring-2	Ground / Common
4	Sleeve	Microphone




ESD



Reserved

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		Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title 030_Audio Jack_(R) (2/2)			
Size A	Document Number LA710		Rev 1
Date:	Monday, April 02, 2018	Sheet	30 of 107

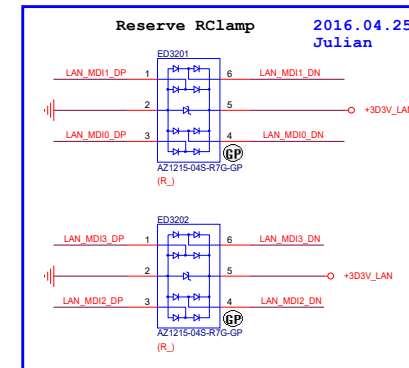
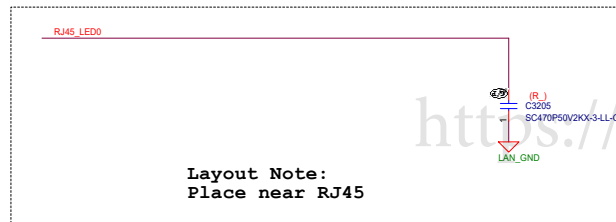
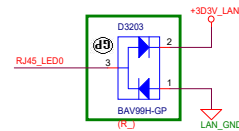
[31] LAN_MDIO_DP
[31] LAN_MDIO_DN

[31] LAN_MD1_DP
[31] LAN_MD1_DN

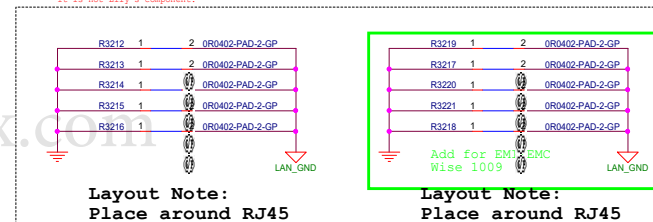
[31] LAN_MD2_DP
[31] LAN_MD2_DN

[31] LAN_MD3_DP
[31] LAN_MD3_DN

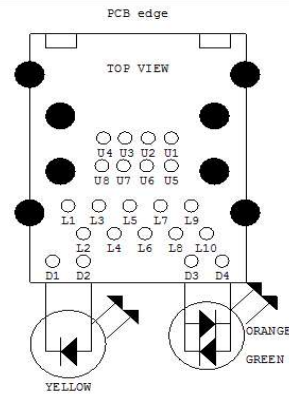
[31] RJ45_LED0



C10 Previous component
78.10324.2FLL: CHIP CAP C 0.01U 50V K0402 X7R
it is not Lilu's component

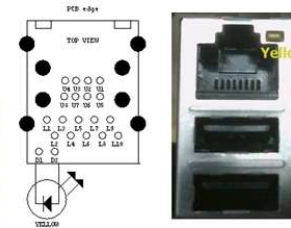


WOL	status	Yellow	Grn/Org
don't care	No Link	off	off
off(IE WOL and Host WOL should be disable both)	S3/S4/S5	off	off
on	10M.inactive		off
on	10M.active		off
on	100M.inactive		
on	100M.active		
on	1G.inactive		
on	1G.active		



RJ45 common spec

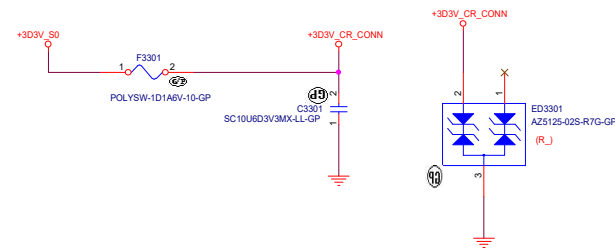
WOL	status	Yellow
don't care	No Link	off
off(ME WOL and Host WOL should be disable both)	S3/S4/S5	off
on	10M_inactive	
on	10M_active	
on	100M_inactive	
on	100M_active	
on	1G_inactive	
on	1G_active	



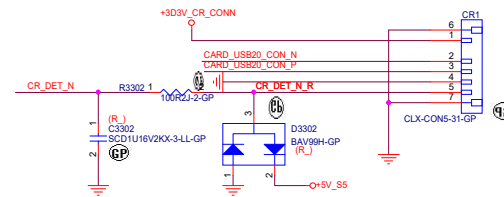
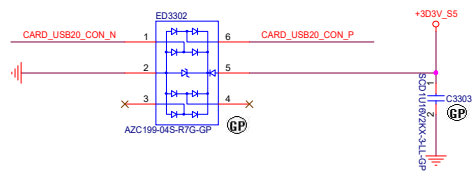
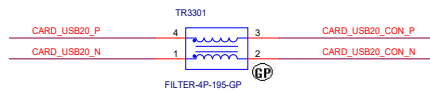
Card Reader

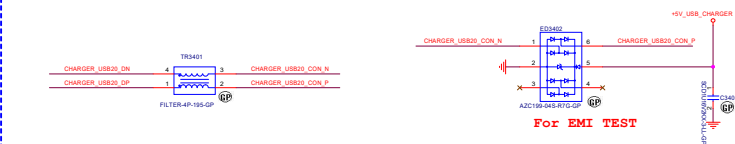
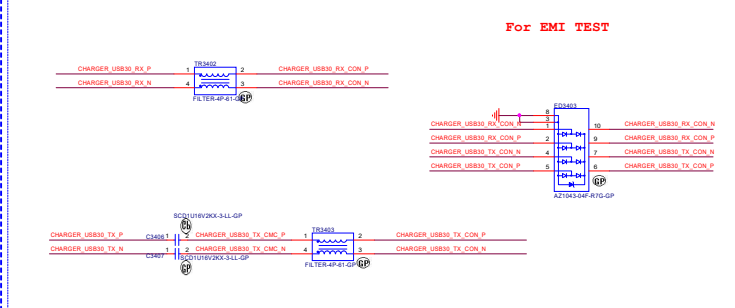
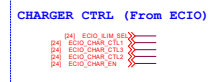
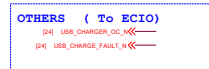
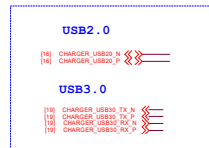
Card Reader

[16] CARD_USB20_N
[16] CARD_USB20_P
[15] CR_DET_N

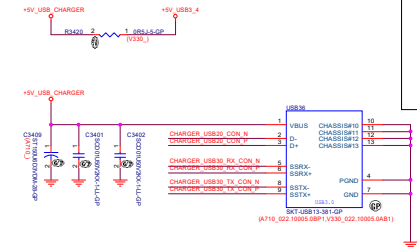


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Front USB3.0 CONNECTOR

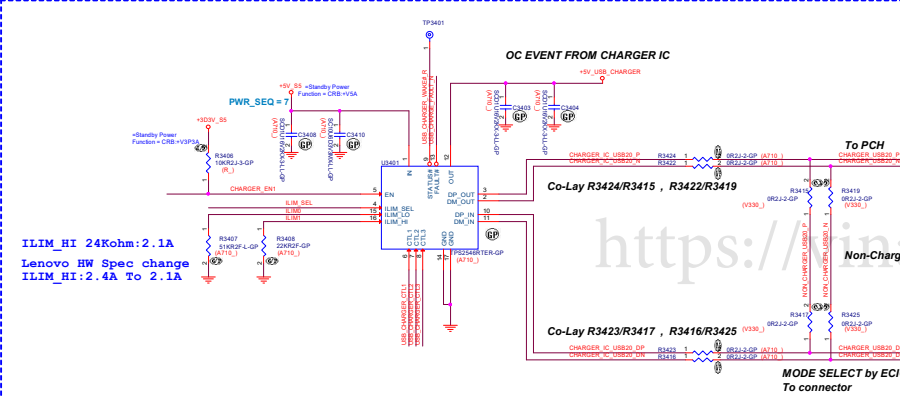


USB 3.0 Connector Pin definition

1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	Std_A_SSRX- SuperSpeed RX
6	Std_A_SSRX+ SuperSpeed RX
7	GND
8	Std_A_SSTX- SuperSpeed TX
9	Std_A_SSTX+ SuperSpeed TX

Control Pin Settings Matched to System Power States

System Global Power State	TPS2546 Charging Mode	CTL1	CTL2	CTL3	ILIM_SEL	Current Limit Setting
S0	CDP, load detection with ILIM_LO + 60mA thresholds or if a BC1.2 primary detection occurs	1	1	1	1	S0: CDP, 1.5A => 1 1 1 1
S4/S5	Auto mode, load detection with power wake thresholds, no mouse wake	0	0	1	1	S4/S5: DCP 1.5A => 0 0 1 1
S3	Auto mode, keyboard/mouse wake up, load detection with ILIM_LO + 60mA thresholds	0	1	1	1	S3: SDP, 0.5A => 0 1 1 1
S3	Auto mode, keyboard/mouse wake-up, no load detection	0	1	1	0	ILIM_HI
S3	SDP, keyboard/mouse wake-up	0	1	0	1 or 0	ILIM_HI / ILIM_LO



1.2 DPM AP Function Control Introduce



6.3 Fault# signal application

Charger IC Fault# would trigger during over-temperature and current limit conditions and the charger IC would reset SMBUS (reset voltage and current) when Portable devices contact with Charger. So it would be erroneous triggered under current-limit and Charger IC discharger conditions.

Suggestion:

6.3.1 Block Diagram



6.3.2 EC control

EC use traditional OC# and Charger IC Fault# to operation program to indicate short condition.
S0: Detect that if IC Fault# signal is triggered, EC assert OC# to PCH.
S3: Detect that traditional OC# and Charger IC fault# are both triggered, EC assert OC# to PCH.

Note:

- 1) All shaded boxes are device charging modes
- 2) See below table for CTL settings corresponding to flow line conditions

Flow Line Condition	CTL1	CTL2	CTL3	ILIM_SEL
DCH	0	0	0	X
CDP	1	1	1	1
SDP2	1	1	1	0
SDP1	1	1	0	X
DCP SHORT	0	1	0	X
DCP DIVIDER	1	0	1	X
DCP_Auto	0	1	1	X
	0	0	1	X

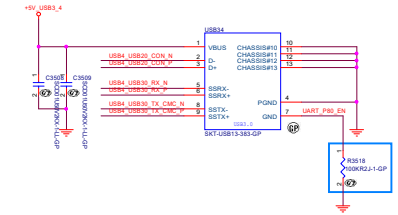
Default status:

ECIO_CHAR_CTL1	ECIO_CHAR_CTL2	ECIO_CHAR_EN	Mode	State
1	1	1	CDP	S0
0	1	1	DCP with HID auto detect USB data pass through	S3
0	0	1	DCP	S4/S5
0	0	0	Shut down	EN DSW and DIS CHARG on S4/S5

Control pin Truth Table Setting

Mode	CTL1	CTL2	CTL3	ILIM_SEL
CDP (S0)	1	1	1	1
DCP (S3)	0	1	1	0
DCP (S4/S5)	0	0	1	1

USB 2.0 **For EMI TEST**



USB 2.0 * 4 ==>

[14] USB1_USB20_N
[14] USB1_USB20_P
[14] USB2_USB20_N
[14] USB2_USB20_P
[14] USB3_USB20_N
[14] USB3_USB20_P
[14] USB4_USB20_N
[14] USB4_USB20_P

USB3.0 * 4 ==>

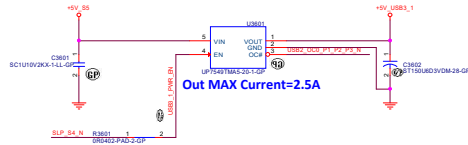
[14] USB1_USB30_TX_P
[14] USB1_USB30_TX_N
[14] USB1_USB30_RX_P
[14] USB1_USB30_RX_N
[14] USB2_USB30_TX_P
[14] USB2_USB30_TX_N
[14] USB2_USB30_RX_P
[14] USB2_USB30_RX_N
[14] USB3_USB30_TX_P
[14] USB3_USB30_TX_N
[14] USB3_USB30_RX_P
[14] USB3_USB30_RX_N
[14] USB4_USB30_TX_P
[14] USB4_USB30_TX_N
[14] USB4_USB30_RX_P
[14] USB4_USB30_RX_N

To PCB USB OC pin

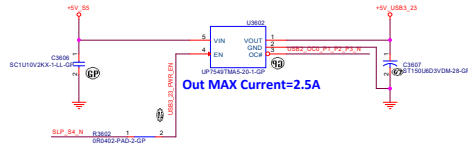
[R3034,R3040] SLP_B4_N
[D4] SMARTPW_EN

BC Control Pin

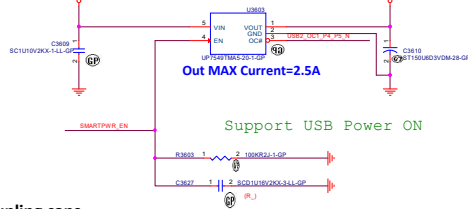
USB PORT1 Power



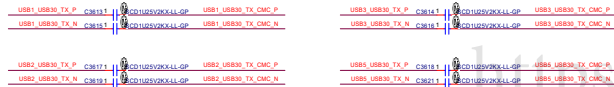
USB PORT2/3 Power



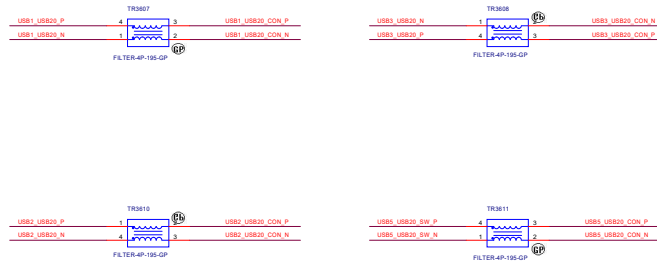
USB PORT5 Power



Coupling caps

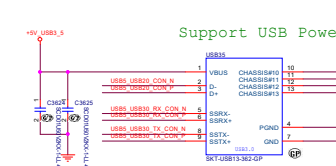
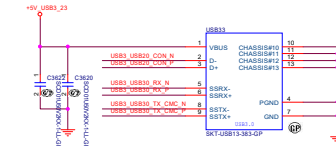
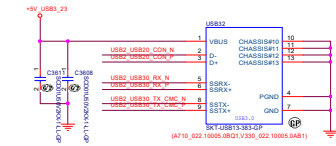
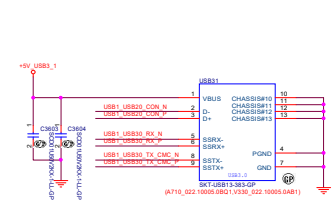
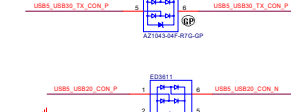
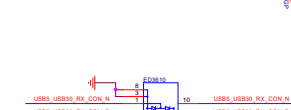
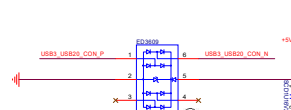
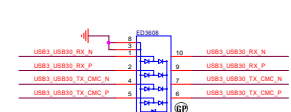
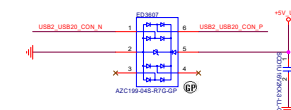
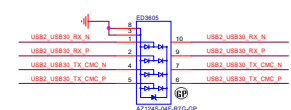
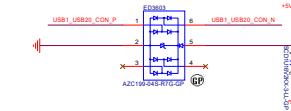
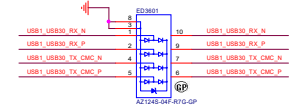


USB 2.0 For EMI TEST



USB3.0

ESD



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037_USB20_(BIOS RECOVERY)_(R)

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Document Number

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Monday, April 02, 2018

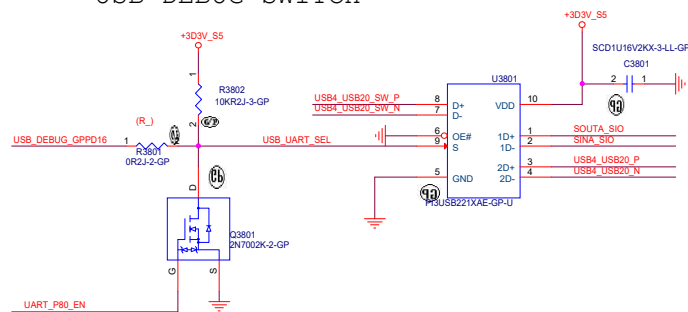
Sheet

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of

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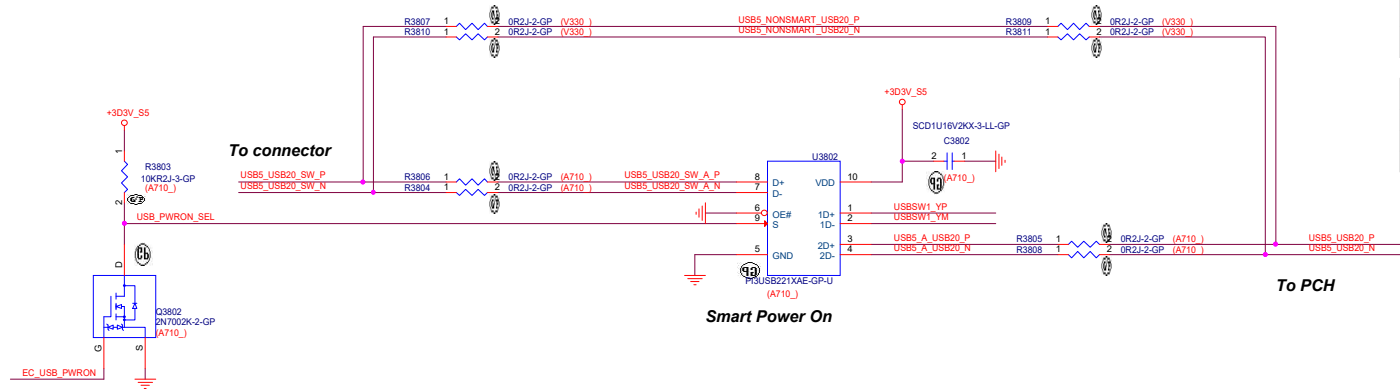
USB DEBUG SWITCH



UART_P80_EN	POST 80	DEBUG CAP
L	DISABLE	NOT INSERT
H	ENABLE	INSERT

OE#	S	FUNCTION
H	X	Disconnect
L	L	D=1D (USB Debug)
L	H	D=2D (USB normal)

Non-Smart Power On



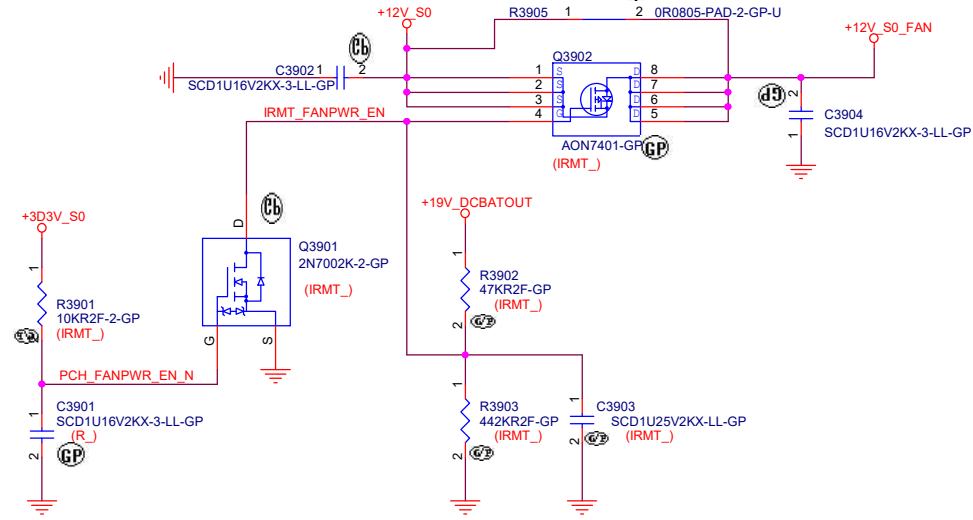
EC_USB_PWRON	PCH USB	EC_USB_PORT
L	PCH - USB CONN	USB Normal (S3/S0)
H	EC - USB CONN	USB smart power on(S5)

OE#	S	FUNCTION
H	X	Disconnect
L	L	D=1D USB power on (S5)
L	H	D=2D USB Normal (S3/S0)

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180402 EE Leon : w/o IRMT => stuff R3905,C3902,C3904

[15] PCH_FANPWR_EN_N >>



[95] SCALAR_PD# <<
[24] EC_EDP_PD_N

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SCALAR_PD# R3904 1 (R_) 0R2J-2-GP EC_EDP_PD_N

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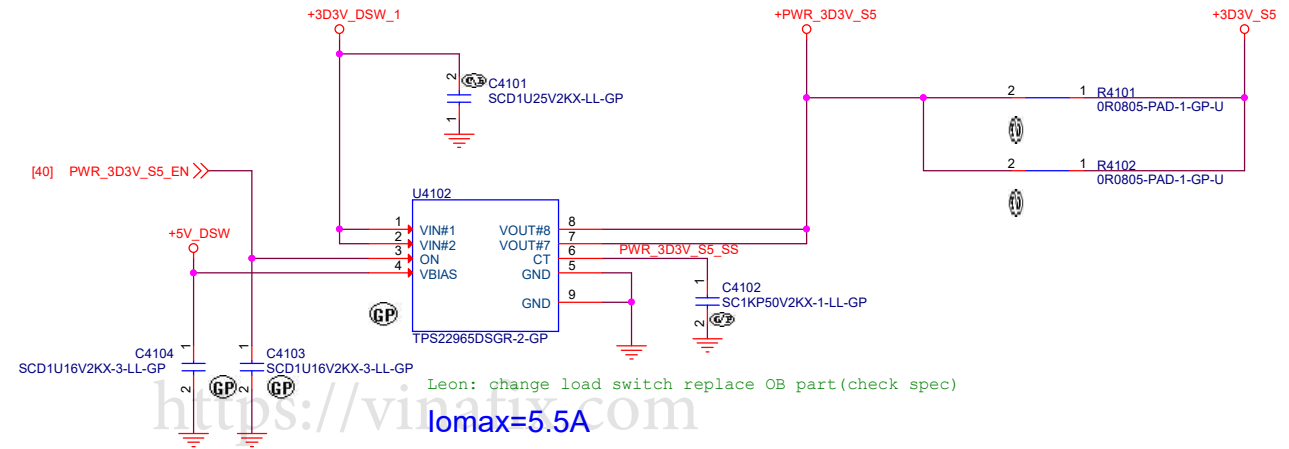
Title
039_IRMT

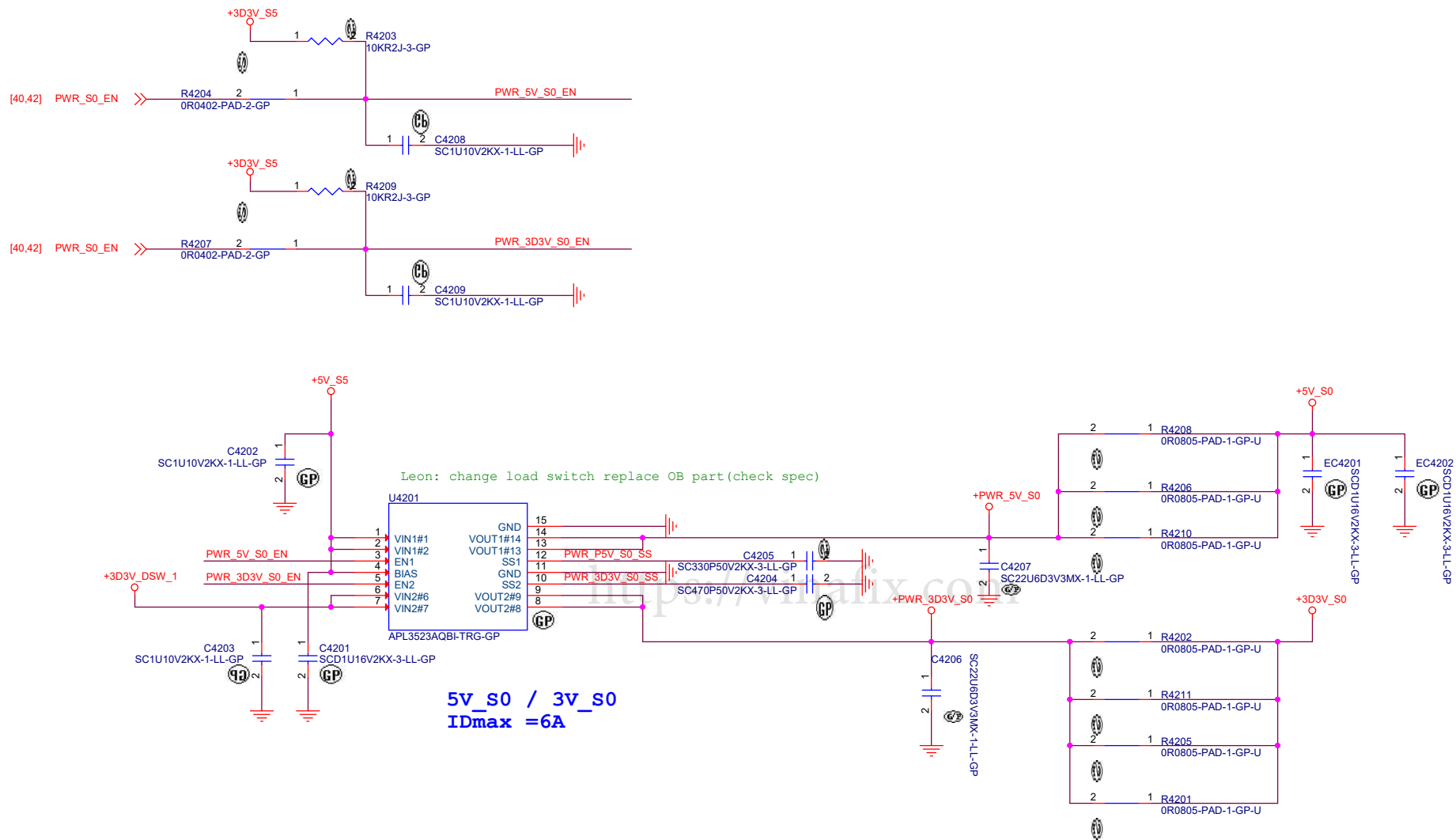
Size B Document Number
LA710


Date: Monday, April 02, 2018

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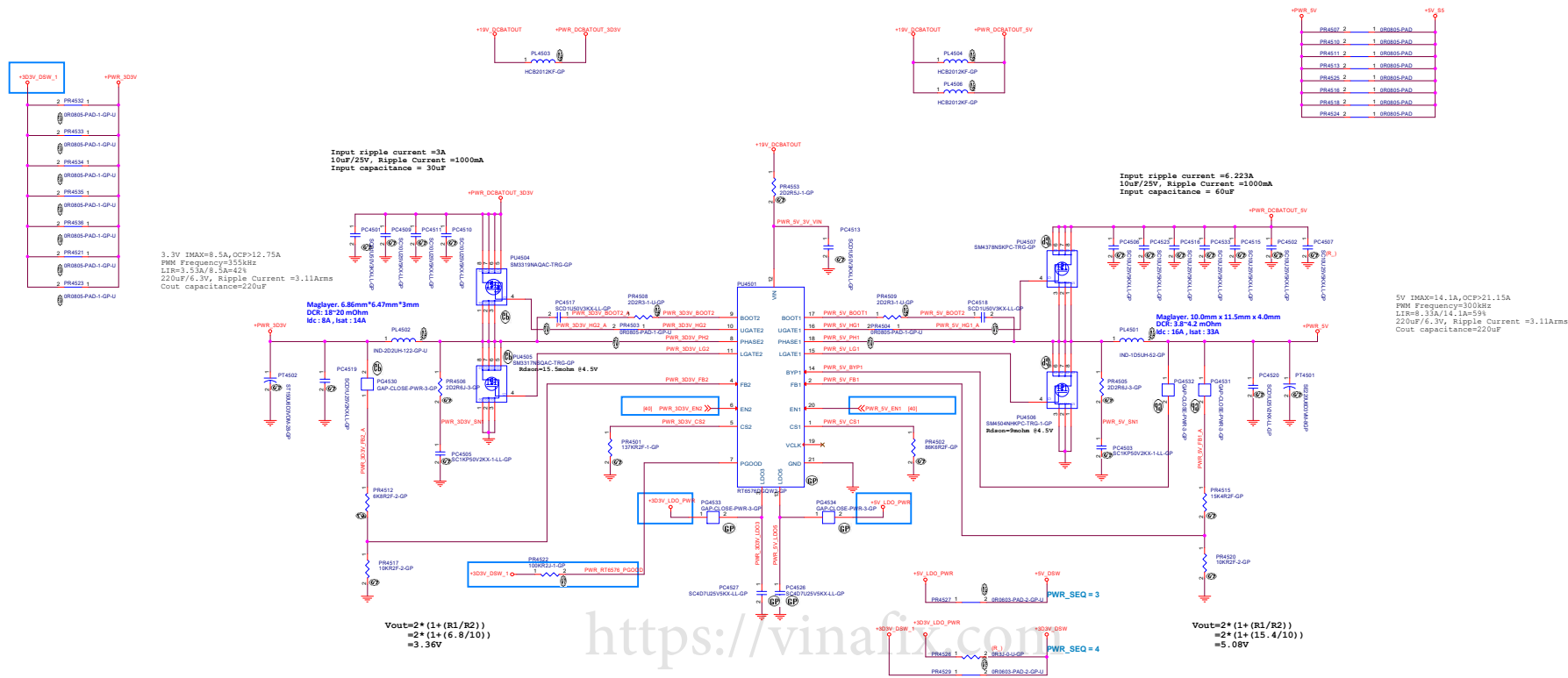
		Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title 042_Switch power_3D3V_S0/5V_S0			
Size B	Document Number LA710		Rev 1
Date: Monday, April 02, 2018	Sheet 42	of 107	

[illegible]

DELAY	ALERT DELAY (μs)
Floating	10uS
GND	50uS
VSS	100uS

	PARAMETER	EQUATION
VTRIP	Desired current trip value	$I_{LOAD} \times R_{SENSE}$
VLIMIT	Programmed threshold limit voltage	$V_{LIMIT} = V_{TRIP}$
VLIMIT(1)	Threshold voltage	$(I_{LIMIT} \times R_{LIMIT}) - NAF$
RLIMIT(1)	Threshold limit setting resistor	$(V_{LIMIT} + NAF) / I_{LIMIT}$
RLIMIT(1)	Limit setting resistor	$(V_{LIMIT} + 500 \mu V) / 20 \mu A$

		Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title: 044 Power meter			
Size: C	Document Number: LA710		Rev: 1
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Table 3. Enabling/PGOOD State (TPS61275B/C)

EN1	EN2	VREG3	VREG3	CH1 (5Vout)	CH2 (3.3Vout)	VCLK	PGOOD
OFF	OFF	ON	ON	OFF	OFF	OFF	Low
ON	OFF	ON	ON	ON	OFF	ON	Low
OFF	ON	ON	ON	OFF	ON	OFF	Low
ON	ON	ON	ON	ON	ON	ON	High

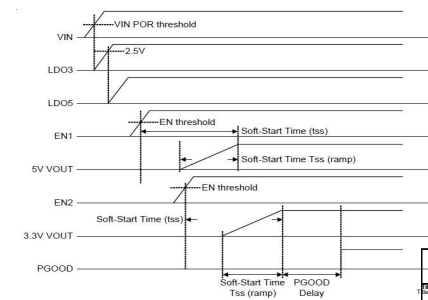
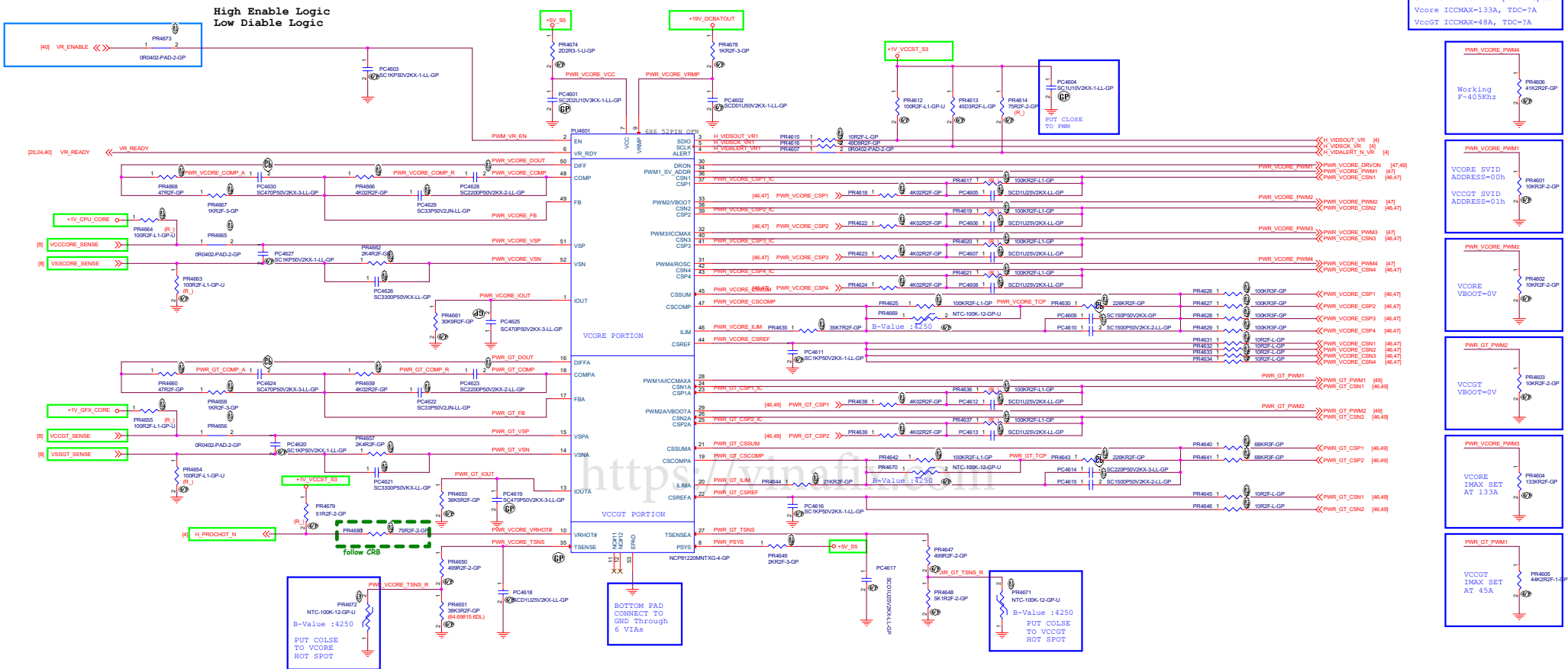


Figure 6. RT8575B Timing

Intel Coffeelake IMVP8 POWER CKT - S-LINE 62 65W 4+2 PHASE



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048_CPU Core_(R)

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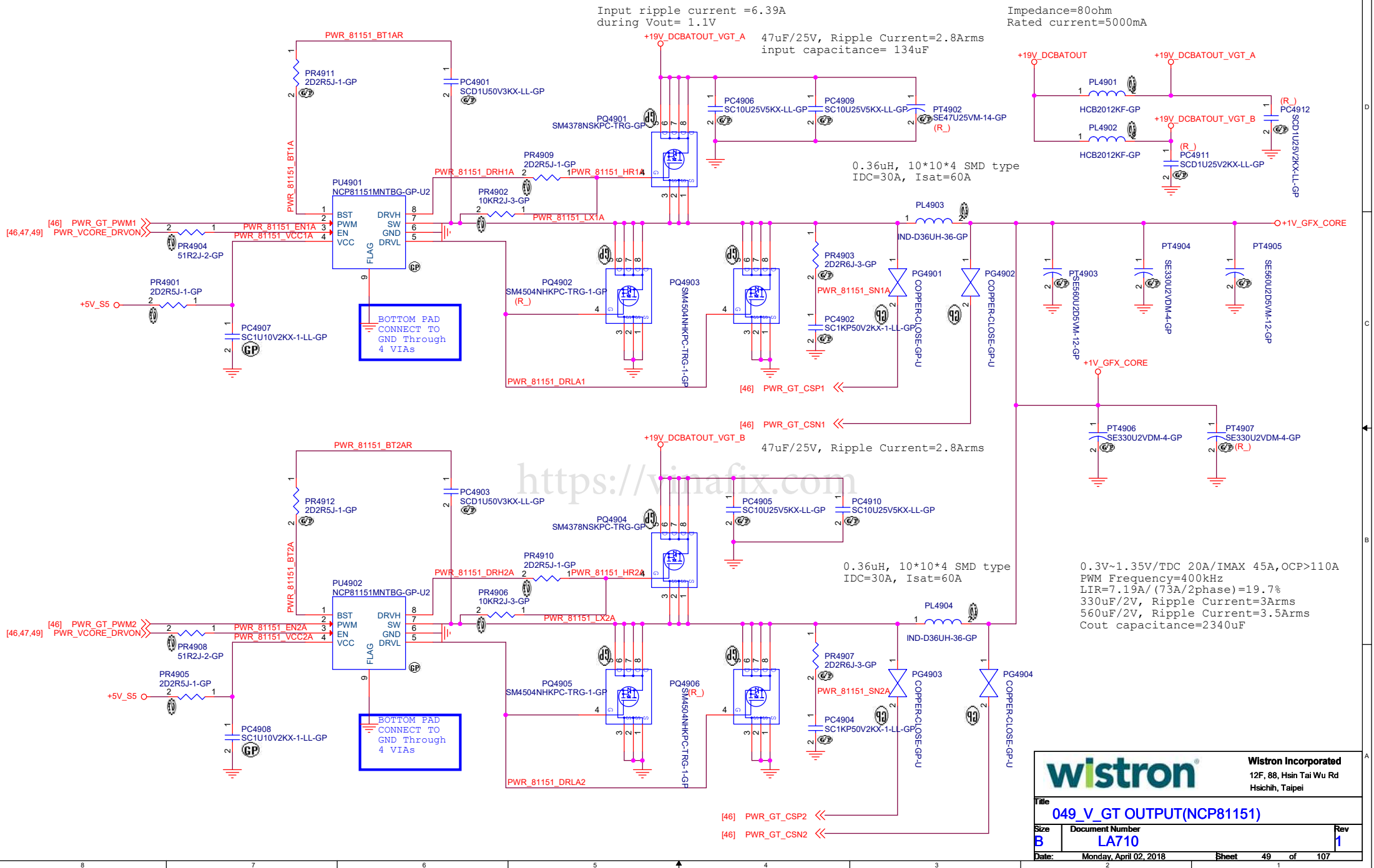
Monday, April 02, 2018

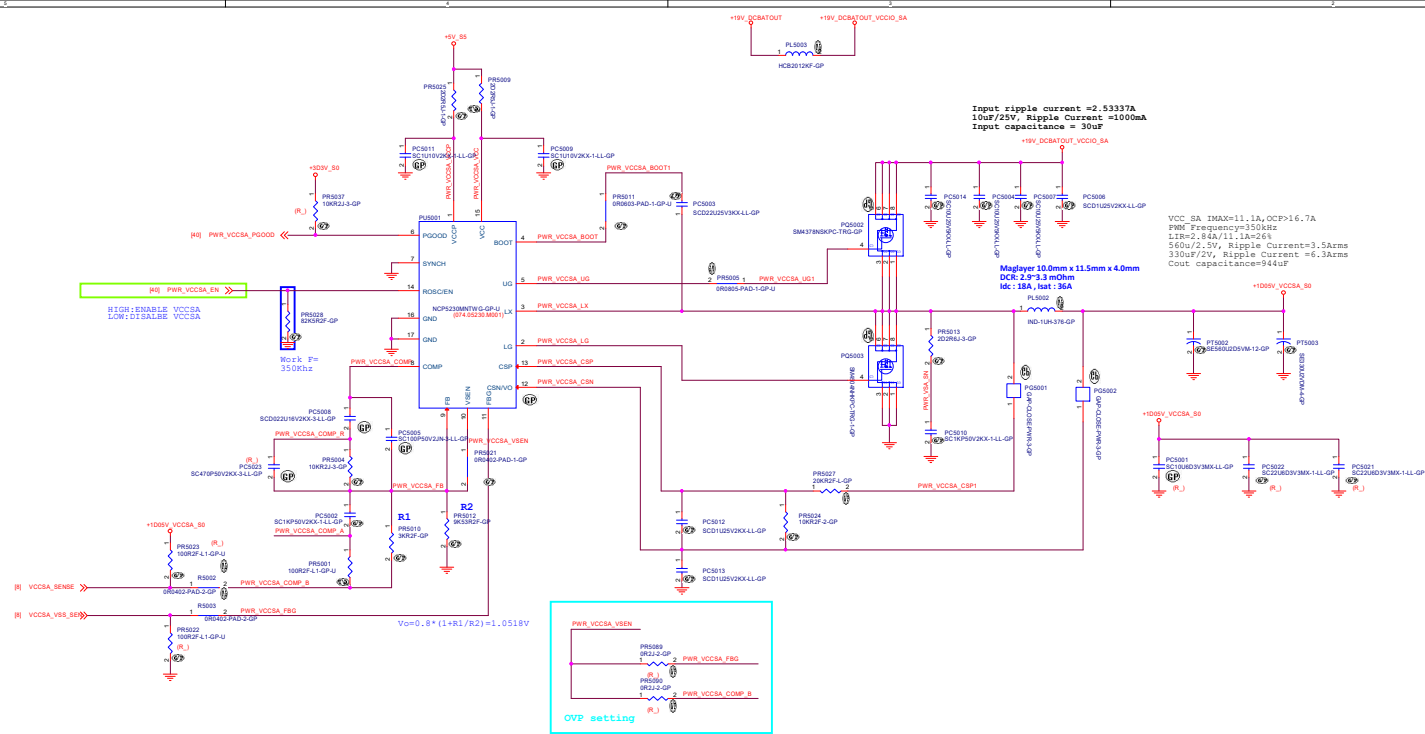
Sheet

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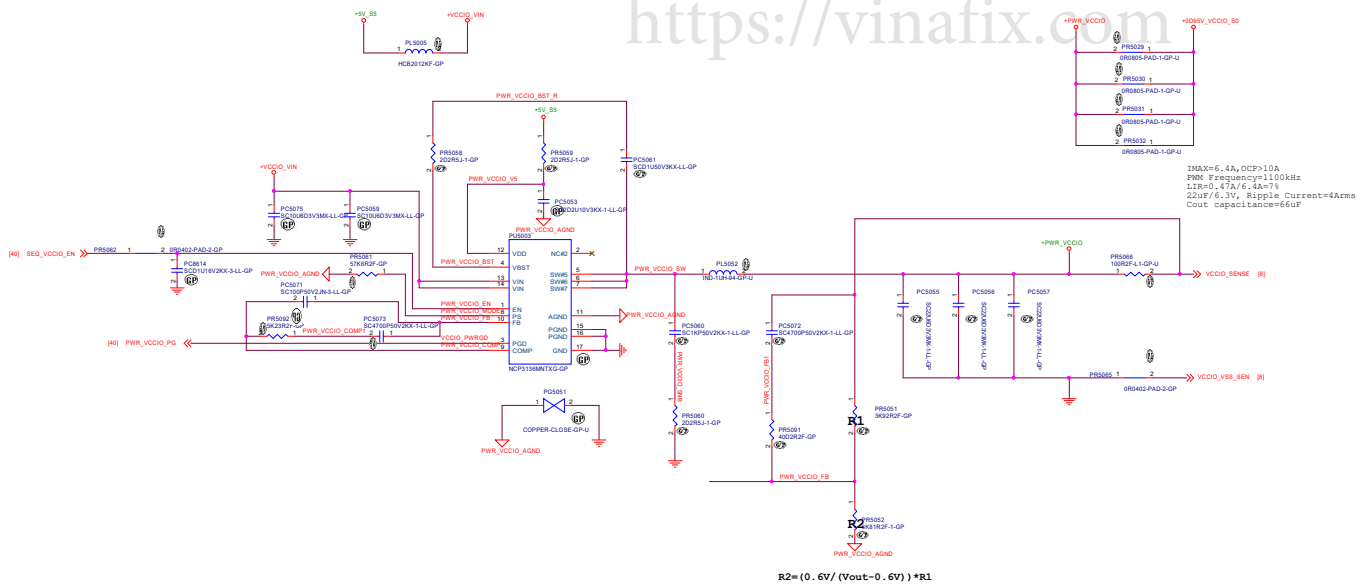
of

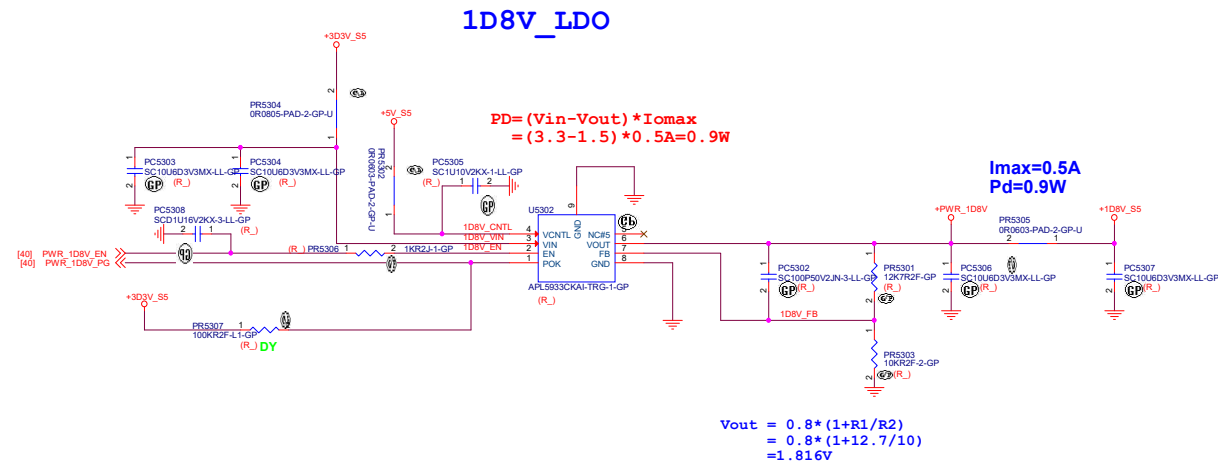
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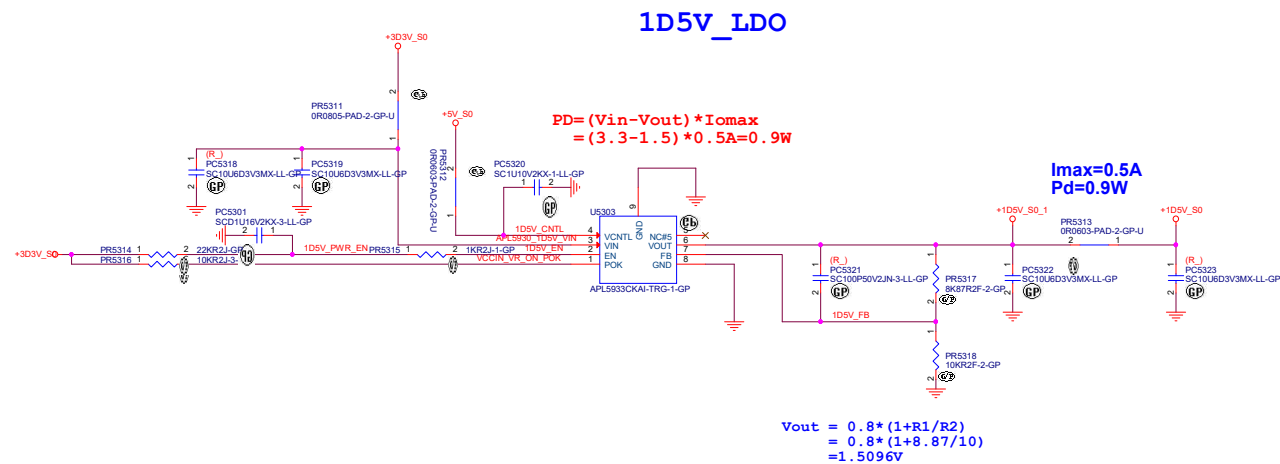


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[95] EDP_TXE3+
[95] EDP_TXE3-
[95] EDP_TXE0+
[95] EDP_TXE0-
[95] EDP_TXE1+
[95] EDP_TXE1-
[95] EDP_TXE2+
[95] EDP_TXE2-
[95] EDP_TXE3+
[95] EDP_TXE3-
[95] EDP_TXE0+
[95] EDP_TXE0-
[95] EDP_TXE1+
[95] EDP_TXE1-
[95] EDP_TXE2+
[95] EDP_TXE2-

[95] EDP_TXO3+
[95] EDP_TXO3-
[95] EDP_TXO0+
[95] EDP_TXO0-
[95] EDP_TXO1+
[95] EDP_TXO1-
[95] EDP_TXO2+
[95] EDP_TXO2-
[95] EDP_TXO3+
[95] EDP_TXO3-
[95] EDP_TXO0+
[95] EDP_TXO0-
[95] EDP_TXO1+
[95] EDP_TXO1-
[95] EDP_TXO2+
[95] EDP_TXO2-

[95] SCALAR_LVDS_BLTEN
[24,95] PS8625_Panel_ON
[24] EC_Panel_ON

[24,64] LCD_ID_0
[24,64] LCD_ID_1
[24,64] LCD_ID_2
[24,64] LCD_ID_3

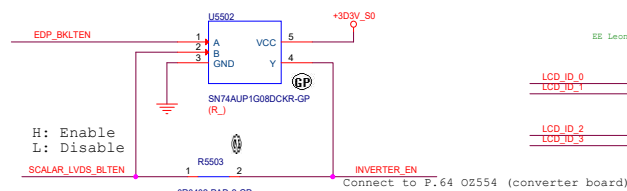
[64] RTN1
[64] RTN2
[64] RTN3
[64] RTN4

[17,24] EDP_BKLTEN

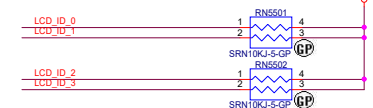
Panel Size 21.5'&20'

Panel Control

[64] INVERTER_EN

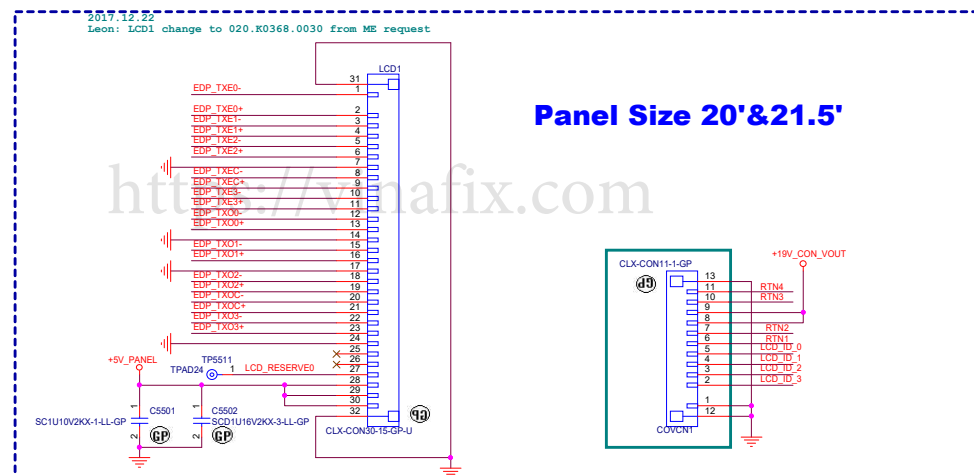


EE Leon: Chang LCD_ID_0-3 power rail from P3V3_S0to P3V3_S5

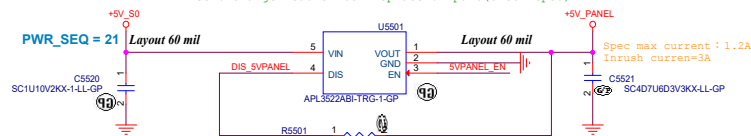


1A 20140311 Darren for EMI

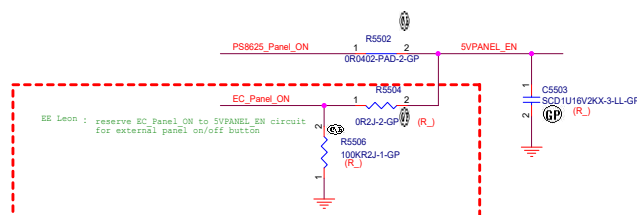
Size	19.5	19.5	19.5
Vendor ID (0x05)			
Panel ID (ID3-ID0)	1110	0111	0011
Vendor	AUO	Innolux	LGD
Panel Mode	M195RTN001.1	M195FGE-L20	LM195WD1
Address			
0x00	11110010	11110010	00110010
0x01	01000011	01000011	01000011
0x02	01011011	01100011	01110011
0x03	00000000	00000000	00000000
0x04	00000000	00000000	00000000
0x05	01001111	00110111	10000111



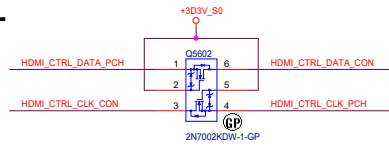
Leon: change load switch replace OB part(check spec)



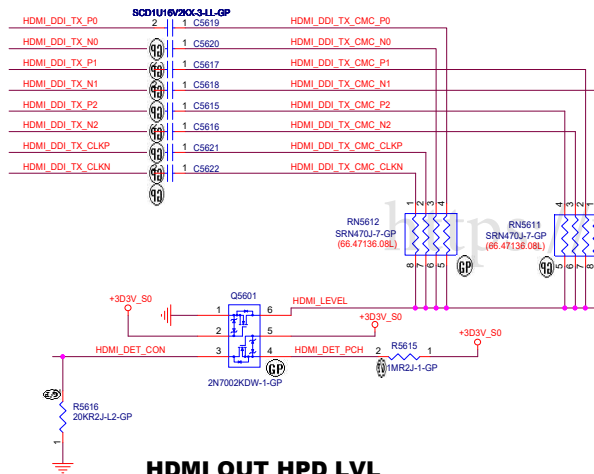
PANEL ON
1: PANEL POWER ON
0: PANEL POWER OFF



HDMI OUT DDC LVL

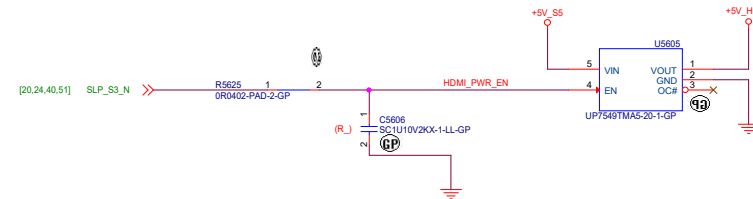
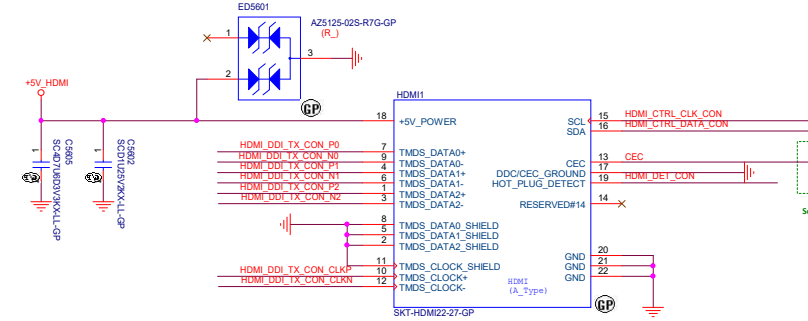
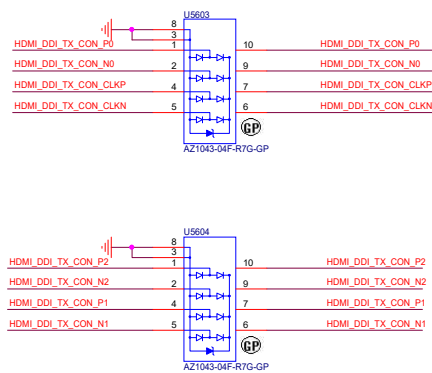


HDMI out Reduced Level Shift

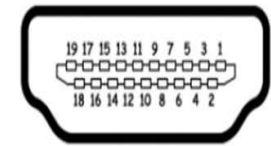
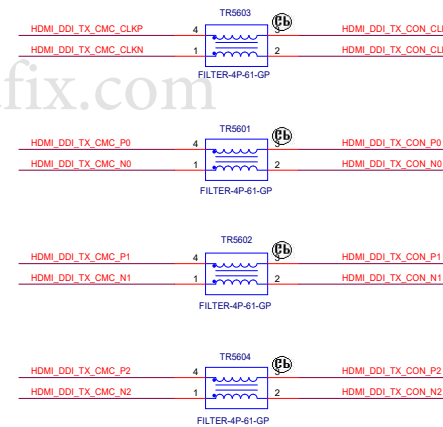


HDMI OUT HPD LVL

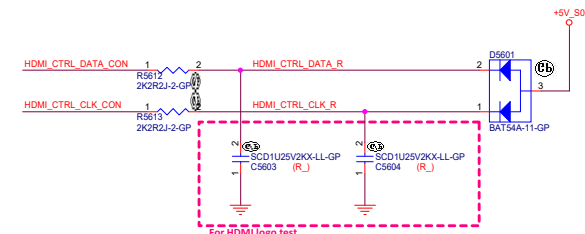
ESD



CMC



Pin#	Signal	Pin#	Signal
1	TMDS data 2+	11	TMDS clock shield
2	TMDS data 2 shield	12	TMDS clock-
3	TMDS data 2-	13	CEC
4	TMDS data 1+	14	No connected
5	TMDS data 1 shield	15	DDC clock
6	TMDS data 1-	16	DDC data
7	TMDS data 0+	17	Ground
8	TMDS data 0 shield	18	+5V power
9	TMDS data 0-	19	Hot plug detect
10	TMDS clock+		



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057_DP_out_(R)

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058_DP_REDRIIVER_(R)

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059_Display switch_(R)

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SATA

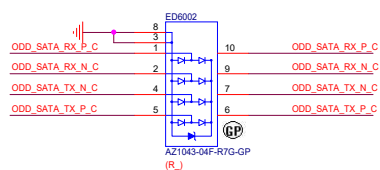
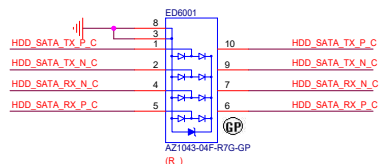
HDD

[17] HDD_SATA_TX_P
[17] HDD_SATA_TX_N
[17] HDD_SATA_RX_P
[17] HDD_SATA_RX_N

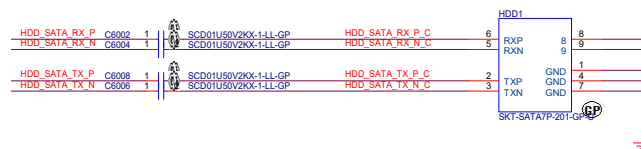
ODD

[17] ODD_SATA_TX_P
[17] ODD_SATA_TX_N
[17] ODD_SATA_RX_P
[17] ODD_SATA_RX_N

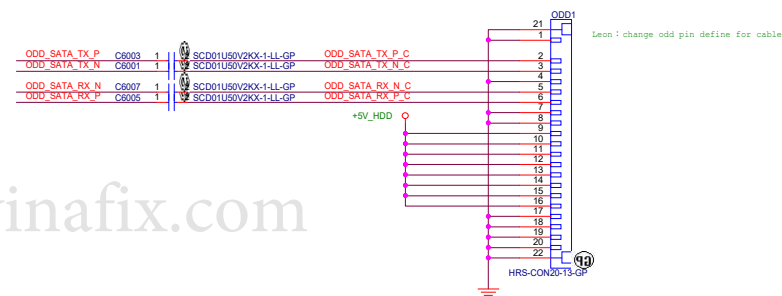
CONN



SATA HDD Connector (Red color)



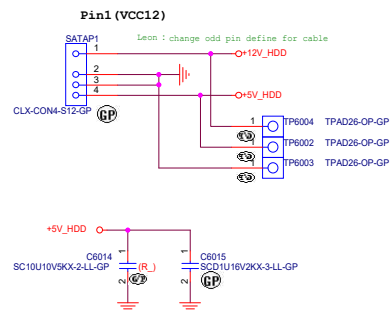
ODD Connector



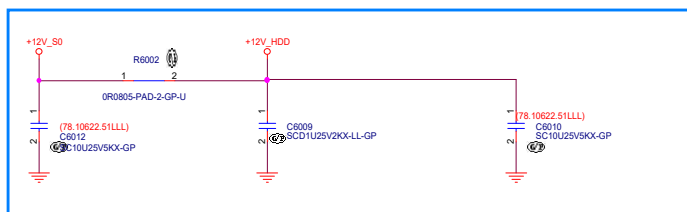
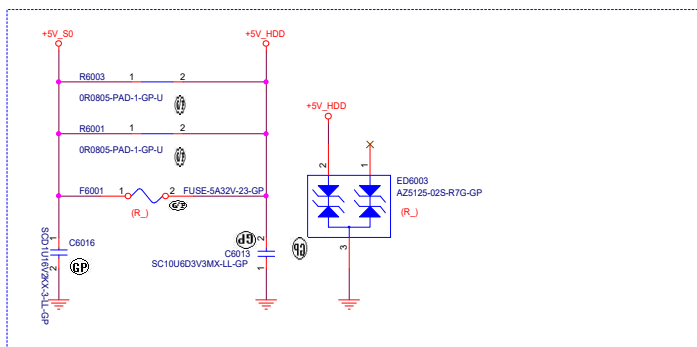
<https://vinafix.com>

SATA

Layout: Please put them together



AC coupling caps near connector<100 mils



20170330 Add 12V_HDD Landis


```
[16] WLAN_PCIE_RX_N
[16] WLAN_PCIE_RX_P
[16] WLAN_PCIE_TX_N
[16] WLAN_PCIE_TX_P
```

[24,31,62] EC_WAKE_N <<—
24,31,68,91,95] EC_RSTOUT0_N >>—

```
[16] WLAN_USB20_N <==>
[16] WLAN_USB20_P <==>
```

```

[20,62] SUSCLK_PCH
[18] WLAN_CLK100M_PCH_N
[18] WLAN_CLK100M_PCH_P

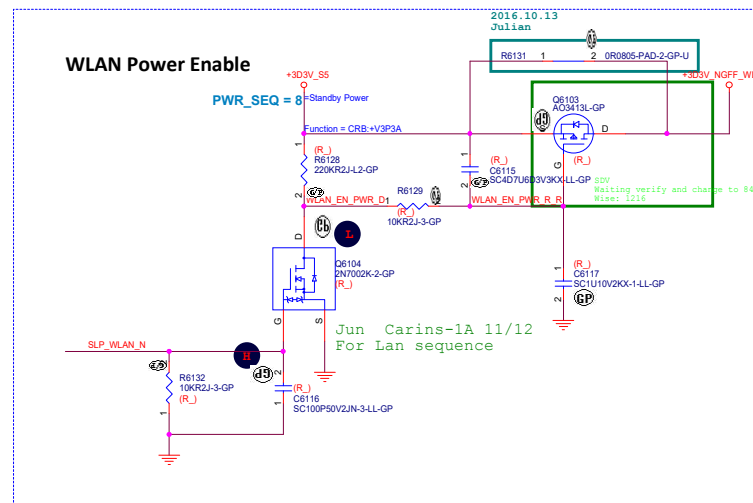
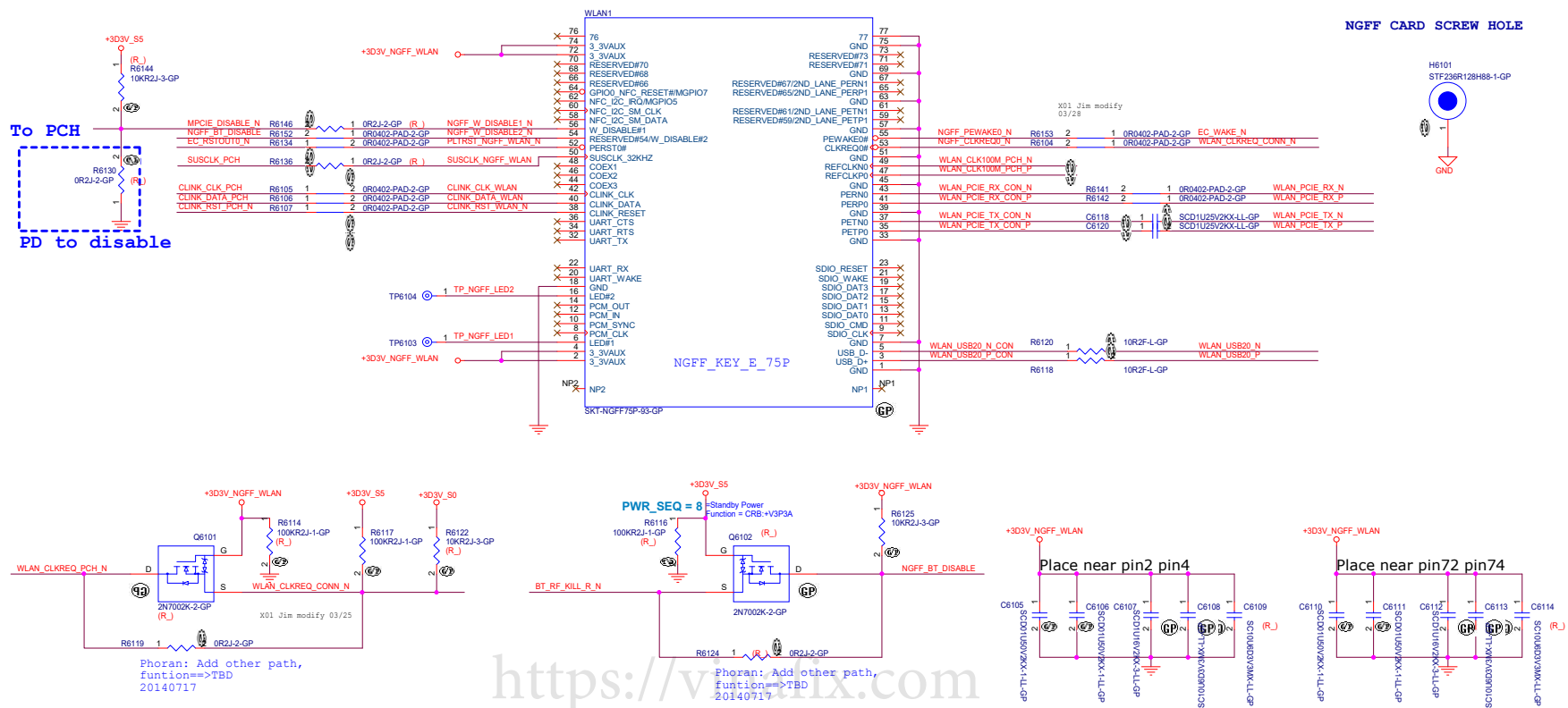
```

```
[16] MPCIE_DISABLE_N
[15] BT_RF_KILL_R_N
[20] SLP_WLAN_N
```

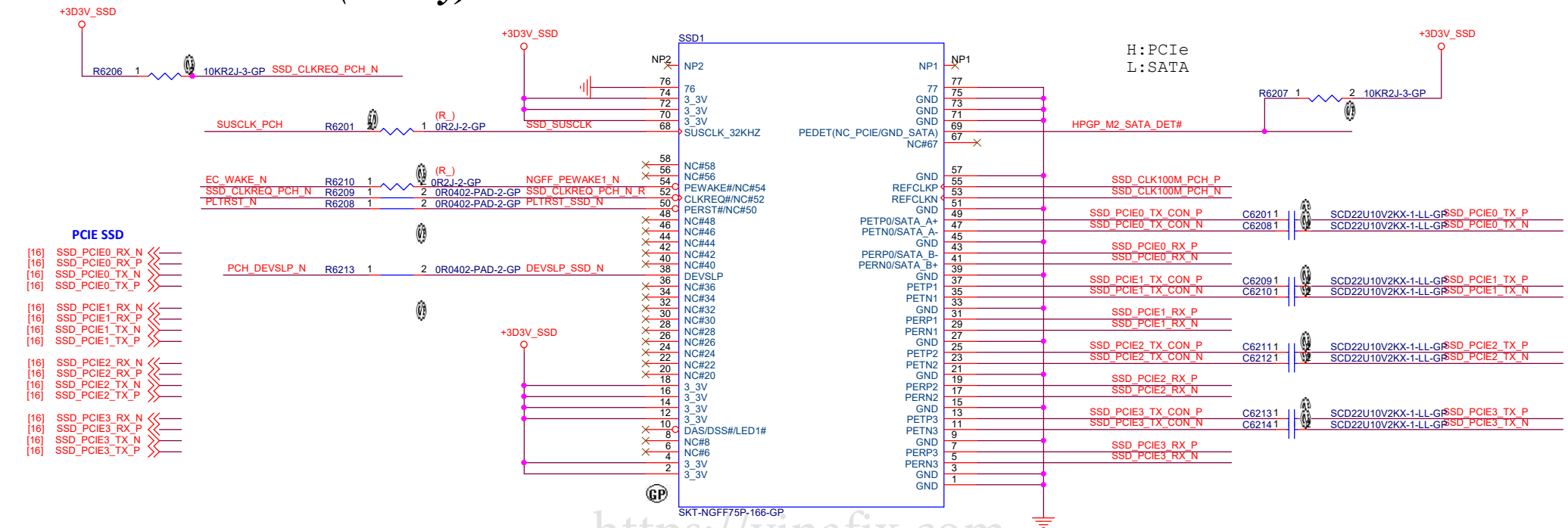
```

[18] WLAN_CLKREQ_PCH_N  <<>>
      [17] CLINK_CLK_PCH  >>>
      [17] CLINK_DATA_PCH >>>
      [17] CLINK_RST_PCH_N >>>

```

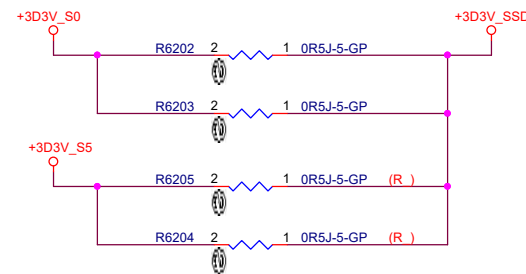
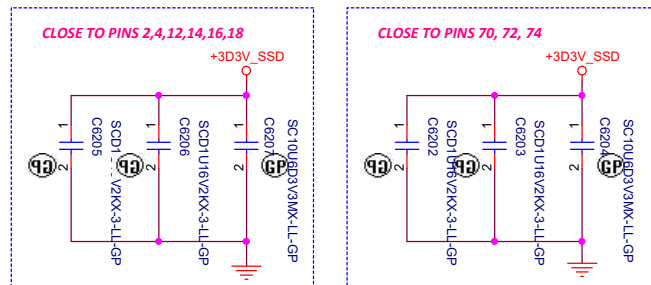
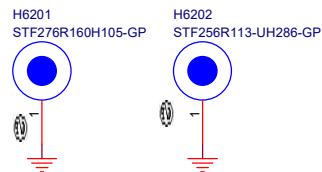


NGFF(M Key)



- [16] SSD_PCIE0_RX_N <<
- [16] SSD_PCIE0_RX_P <<
- [16] SSD_PCIE0_TX_N <<
- [16] SSD_PCIE0_TX_P <<
- [16] SSD_PCIE1_RX_N <<
- [16] SSD_PCIE1_RX_P <<
- [16] SSD_PCIE1_TX_N <<
- [16] SSD_PCIE1_TX_P <<
- [16] SSD_PCIE2_RX_N <<
- [16] SSD_PCIE2_RX_P <<
- [16] SSD_PCIE2_TX_N <<
- [16] SSD_PCIE2_TX_P <<
- [16] SSD_PCIE3_RX_N <<
- [16] SSD_PCIE3_RX_P <<
- [16] SSD_PCIE3_TX_N <<
- [16] SSD_PCIE3_TX_P <<
- [18] SSD_CLK100M_PCH_N <<
- [18] SSD_CLK100M_PCH_P <<
- [18] SSD_CLKREQ_PCH_N <<
- [18] SSD_CLKREQ_PCH_P <<
- [15,24] PLTRST_N >>
- [24,31,61] EC_WAKE_N <<
- [17] HP GP_M2_SATA_DET# <<
- [20,61] SUSCLK_PCH >>
- [19] PCH_DEVSLP_N >>

170504 Leon : Check stand off location



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Title: 062_M.2 card-SSD			
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063_Mini card-NGFF_(R)

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[24] EC_PANSWH_N
[24] PANEL_ON_OFF

[15] BRIGHTNESS_PLUS
[15] BRIGHTNESS_MINUS

[24] B_R15#
 [24] B_CTS15#
 [24] B_RTS15#
 [24] B_DSR15#
 [24] B_DCD15#
 [24] B_RXD1
 [24] B_DTR1#
 [24] G_ZVH1#

[15] CAM_DET_N <<—

[16] WEBCAM_USB20_N <<<<—

[16] WEBCAM_USB20_P <<<<—

[24] EC_SUS_LED >>—

The schematic diagram illustrates the power and brightness control circuit. It features a power supply section with a 30V SW input, a 100nF capacitor, and a 100k resistor. The brightness control section includes a 100k resistor, a 100nF capacitor, and a 100k resistor. The output section shows the connection to the panel, including the panel on/off control, brightness plus/minus controls, and the panel on/off control signal.

[illegible]

Power LED Behavior Define	
Power State	LED Behavior
S0(System on)	On(Always)
S3(System in Standby)	Gradual 1s On, Gradual 1s Off, 3s OFF
S4(System entering hibernation)	Blink (0.25 s On/ 0.25 s Off)
S5(System off)	OFF
G3-S5(Initial Connector of Power) (e.g. via AC adaptor or AC-in)	Blink 3 Times (0.25 s On/ 0.25 s Off , repeat x 3)


[illegible][illegible][illegible]

170828 Leon:Change BTN1 to 020.K0308.0004 for SB

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<Variant Name>

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Title 066_HDMI Redriver_(R)			
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Title

067_THERMAL SENSOR HEAD_(R)

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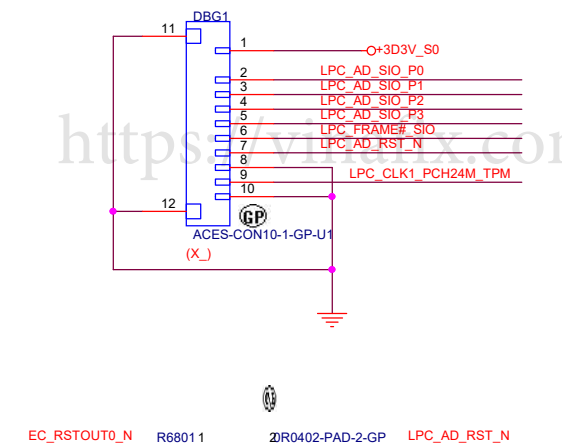
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LPC DEBUG PORT

[19,24,91] LPC_AD_SIO_P0<<<
[19,24,91] LPC_AD_SIO_P1<<<
[19,24,91] LPC_AD_SIO_P2<<<
[19,24,91] LPC_AD_SIO_P3<<<
[19,24,91] LPC_FRAME#_SIO <<<
[19,91] LPC_CLK1_PCH24M_TPM <<<
[24,31,61,91,95] EC_RSTOUT0_N <<<



wistron		Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title 068_Debug_LPC			
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069_4K Panel_(R)

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070_G Sensor_(R)

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071_Thunderbolt_(1/5)_(R)

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072_Thunderbolt_(2/5)_(R)

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073_Thunderbolt_(3/5)_(R)

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074_Thunderbolt_(4/5)_(R)

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075_Thunderbolt_(5/5)_(R)

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076_GPU_function (1/5)_(R)

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077_GPU_function (2/5)_(R)

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078_GPU_function (3/5)_(R)

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079_GPU_function (4/5)_(R)

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080_GPU_function (5/5)_(R)

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081_GPU VRAM_1,2 (1/4)_(R)

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083_GPU VRAM_5,6 (3/4)

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084_GPU VRAM_7,8 (4/4)

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085_GPU CORE_(solution)_(R)

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086_GPU discrete power_(R)

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087_GPU Switch_(1/2)_(R)

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088_GPU Switch_(2/2)_(R)

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089_GPU_EESwitchSEQ_OPTIMUS_(R)

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090_NFC_(R)

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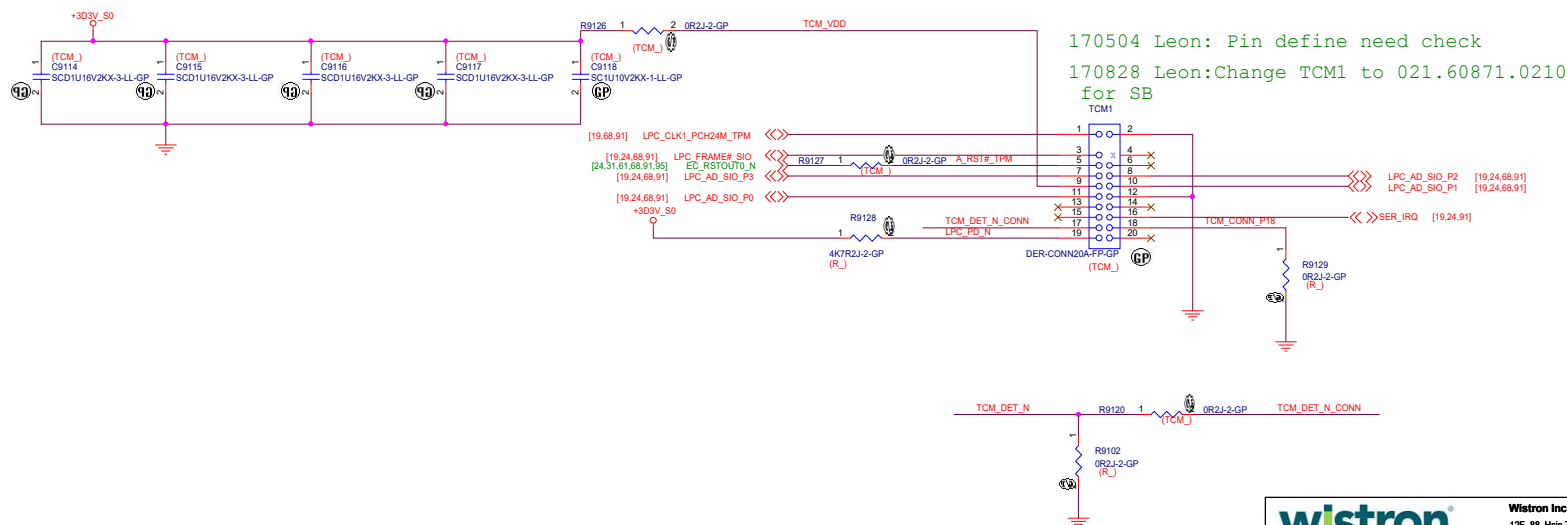
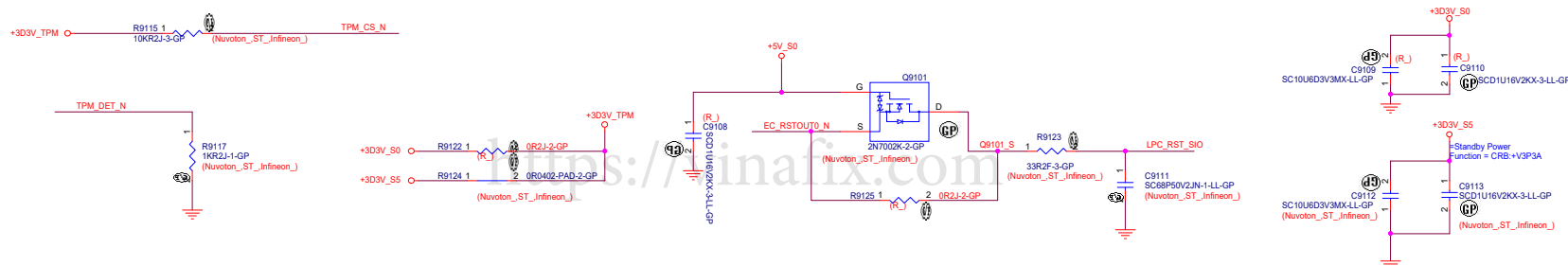
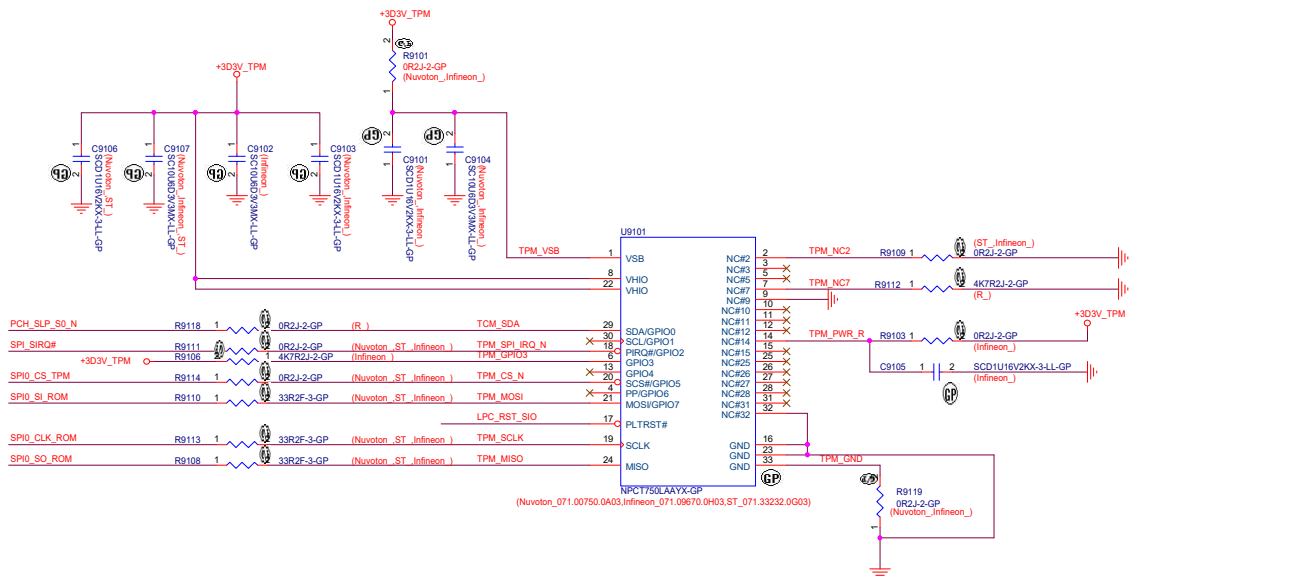
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```

[15]      TPM_DET_N      <<—
[19,24,68,91]  LPC_FRAME#_SIO  <<—

[19,24,91]  SER_IRQ      >>—
[24,31,61,68,91,95]  EC_RSTOUT0_N  >>—
[19,68,91]  LPC_CLK1_PCH24M_TPM  >>—

```



```

[19,68,91] LPC_CLK1_PCH24M_TPM <<>
[19,24,68,91] LPC_FRAME#_SIO <<>
[19,24,68,91] LPC_AD_SIO_P0 <<>
[19,24,68,91] LPC_AD_SIO_P1 <<>
[19,24,68,91] LPC_AD_SIO_P2 <<>
[19,24,68,91] LPC_AD_SIO_P3 <<>
[19,24,91] SER_IRQ <<>
[24,31,61,68,91,95] EC_RSTOUTQ_N <<>
[19] LPC_PD_N <<>
[15] TCM_DET_N <<>

```

[24] MSE_CONN_CLK

[24] MSE_CONN_DAT

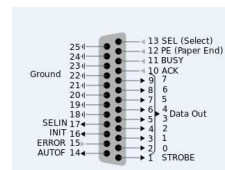
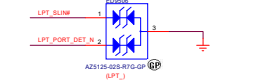
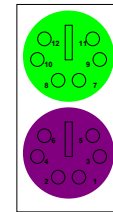
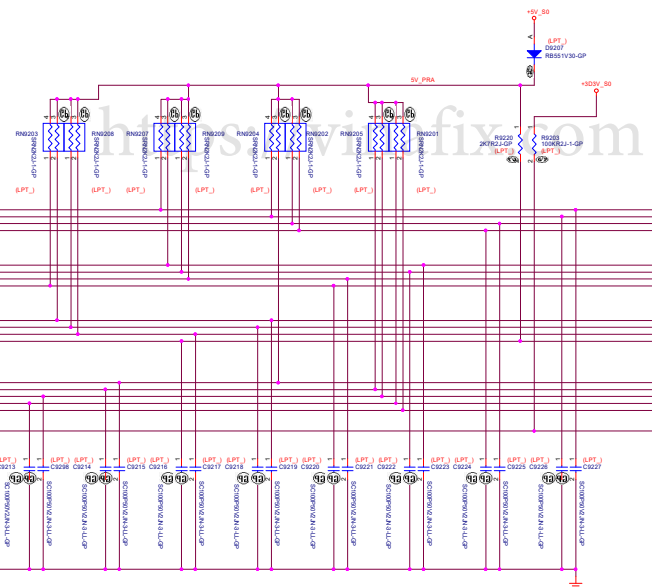
[24] KBD_CONN_DAT

[24] KBD_CONN_CLK

[15] PS2_DET_N




15) LPT_PORT_DET_N <<————



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Title 093_Express Card_(R)			
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094_Smart Card_(R)

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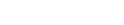
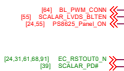
TO LVDS CONN



FROM CPU eDP

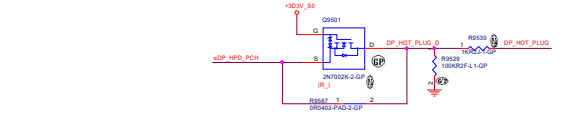


ECIO

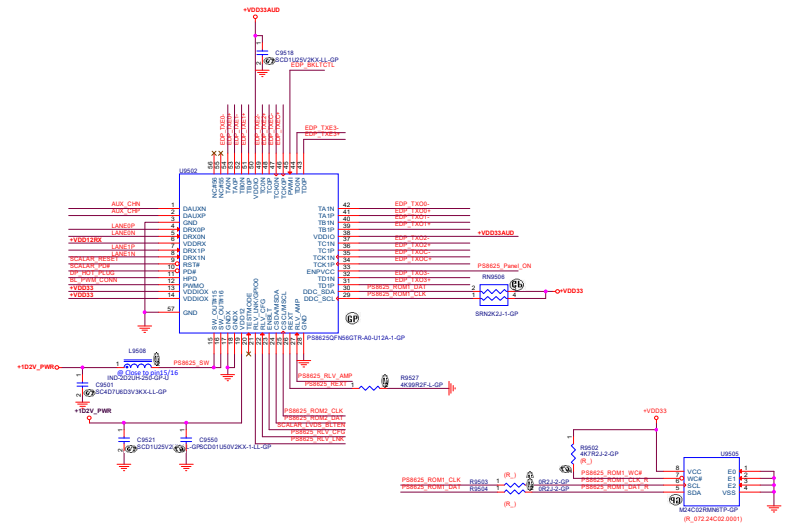


FROM CPU PORT D Main Link

FROM PCH PORT D AUX CH- Link/Device/HPD

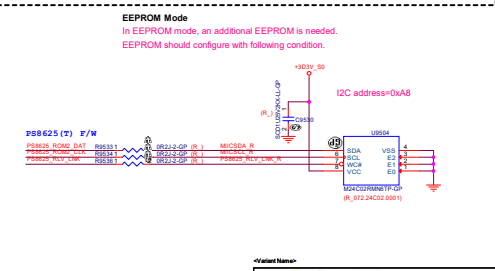
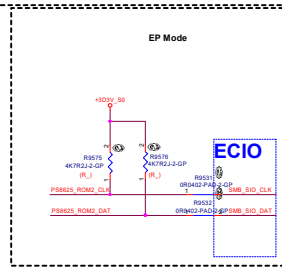
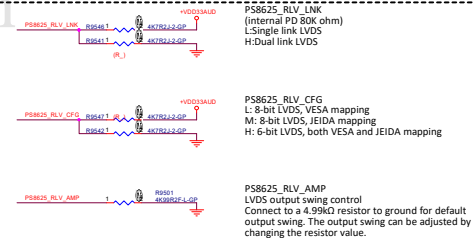


TRANSLATER PS8625 PN:071.08625.003



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Mode Configure Table(Power On Latch)



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096_MCU_(R)

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097_Intel LAN_(R)

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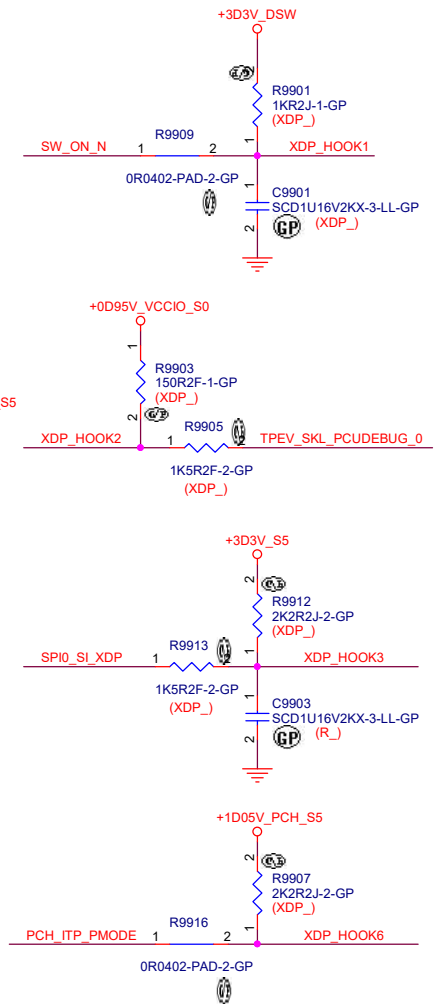
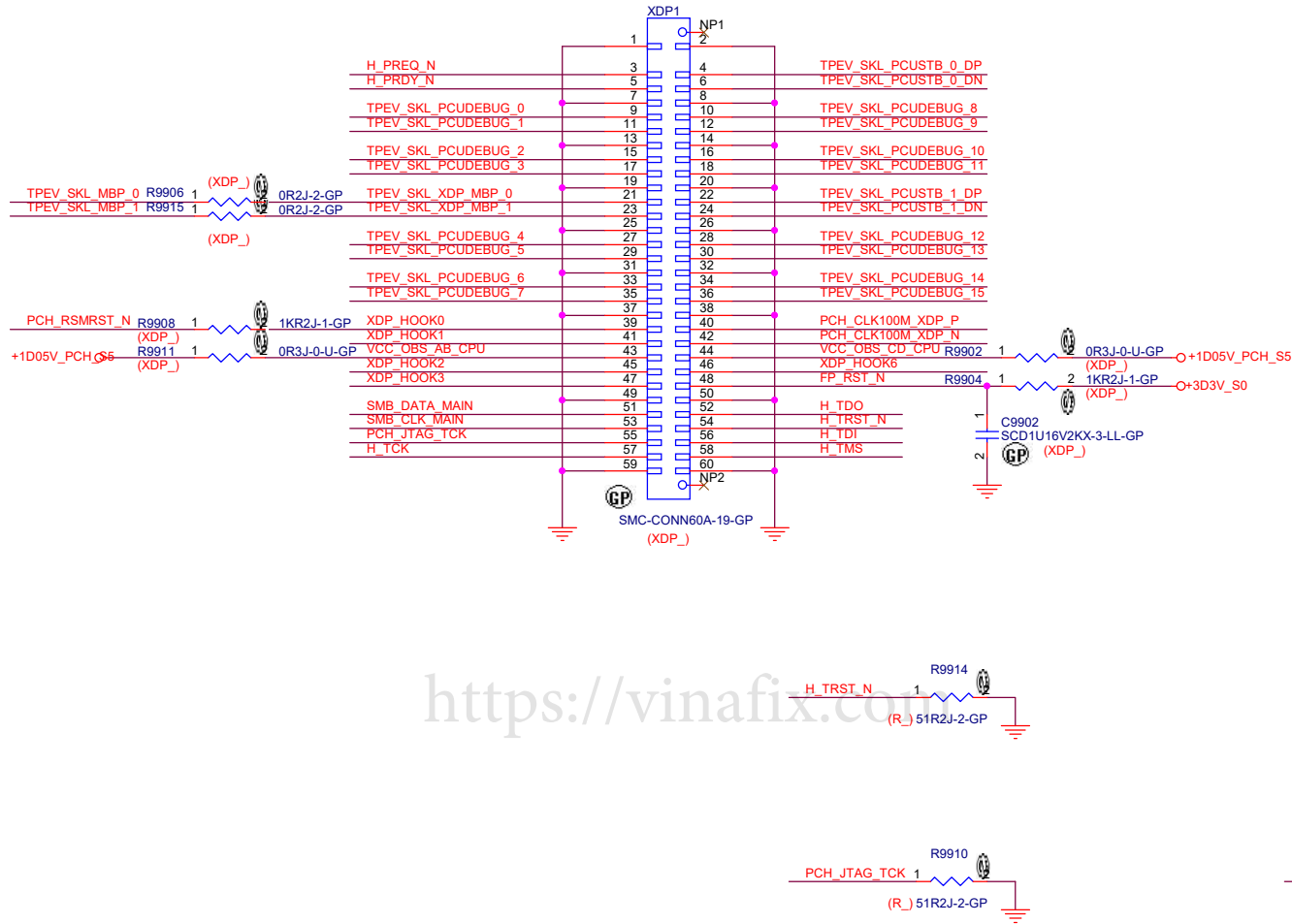
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	5	4	3	2	1
D					D
C					C
B					B
A					A
	5	4	3	2	1


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XDP (PCH)




LABEL




LBL1
LABEL
(40.3KR24.011)




LBL2
LABEL
(R_)



LBL3
LABEL
(R_)



LBL4
LABEL
(R_45.3E702.001)



LBL5
LABEL
(R_45.AGA01.011)

SN LBL

40.3KR24.011 -> 30 x (10+7)mm => for L6

40.3BZ24.011 -> 30x15mm => for L10

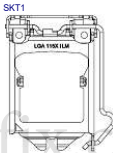
For MP

For CTN LBL

Battery Symbol



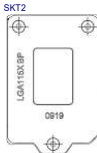
BTT2
BATTERY CR2032
(23.20023.001)



Load Plate
(22.70001.0101)

Second source:

022.70001.0511



Back Plate
(22.78005.011)

Second source:

0022.70001.0121



ILMCOVER
(22.78005.281)

Second source:

22.78005.171

[illegible]

Nuvoton 6858D GPIO Table										
Client Interface										
Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	
GPIO0	0	GPIO1	1	GPIO2	2	GPIO3	3	GPIO4	4	
GPIO5	5	GPIO6	6	GPIO7	7	GPIO8	8	GPIO9	9	
GPIO10	10	GPIO11	11	GPIO12	12	GPIO13	13	GPIO14	14	
GPIO15	15	GPIO16	16	GPIO17	17	GPIO18	18	GPIO19	19	
GPIO20	20	GPIO21	21	GPIO22	22	GPIO23	23	GPIO24	24	
GPIO25	25	GPIO26	26	GPIO27	27	GPIO28	28	GPIO29	29	
GPIO30	30	GPIO31	31	GPIO32	32	GPIO33	33	GPIO34	34	
GPIO35	35	GPIO36	36	GPIO37	37	GPIO38	38	GPIO39	39	
GPIO40	40	GPIO41	41	GPIO42	42	GPIO43	43	GPIO44	44	
GPIO45	45	GPIO46	46	GPIO47	47	GPIO48	48	GPIO49	49	
GPIO50	50	GPIO51	51	GPIO52	52	GPIO53	53	GPIO54	54	
GPIO55	55	GPIO56	56	GPIO57	57	GPIO58	58	GPIO59	59	
GPIO60	60	GPIO61	61	GPIO62	62	GPIO63	63	GPIO64	64	
GPIO65	65	GPIO66	66	GPIO67	67	GPIO68	68	GPIO69	69	
GPIO70	70	GPIO71	71	GPIO72	72	GPIO73	73	GPIO74	74	
GPIO75	75	GPIO76	76	GPIO77	77	GPIO78	78	GPIO79	79	
GPIO80	80	GPIO81	81	GPIO82	82	GPIO83	83	GPIO84	84	
GPIO85	85	GPIO86	86	GPIO87	87	GPIO88	88	GPIO89	89	
GPIO90	90	GPIO91	91	GPIO92	92	GPIO93	93	GPIO94	94	
GPIO95	95	GPIO96	96	GPIO97	97	GPIO98	98	GPIO99	99	
GPIO100	100	GPIO101	101	GPIO102	102	GPIO103	103	GPIO104	104	
GPIO105	105	GPIO106	106	GPIO107	107	GPIO108	108	GPIO109	109	
GPIO110	110	GPIO111	111	GPIO112	112	GPIO113	113	GPIO114	114	
GPIO115	115	GPIO116	116	GPIO117	117	GPIO118	118	GPIO119	119	
GPIO120	120	GPIO121	121	GPIO122	122	GPIO123	123	GPIO124	124	
GPIO125	125	GPIO126	126	GPIO127	127	GPIO128	128	GPIO129	129	
GPIO130	130	GPIO131	131	GPIO132	132	GPIO133	133	GPIO134	134	
GPIO135	135	GPIO136	136	GPIO137	137	GPIO138	138	GPIO139	139	
GPIO140	140	GPIO141	141	GPIO142	142	GPIO143	143	GPIO144	144	
GPIO145	145	GPIO146	146	GPIO147	147	GPIO148	148	GPIO149	149	
GPIO150	150	GPIO151	151	GPIO152	152	GPIO153	153	GPIO154	154	
GPIO155	155	GPIO156	156	GPIO157	157	GPIO158	158	GPIO159	159	
GPIO160	160	GPIO161	161	GPIO162	162	GPIO163	163	GPIO164	164	
GPIO165	165	GPIO166	166	GPIO167	167	GPIO168	168	GPIO169	169	
GPIO170	170	GPIO171	171	GPIO172	172	GPIO173	173	GPIO174	174	
GPIO175	175	GPIO176	176	GPIO177	177	GPIO178	178	GPIO179	179	
GPIO180	180	GPIO181	181	GPIO182	182	GPIO183	183	GPIO184	184	
GPIO185	185	GPIO186	186	GPIO187	187	GPIO188	188	GPIO189	189	
GPIO190	190	GPIO191	191	GPIO192	192	GPIO193	193	GPIO194	194	
GPIO195	195	GPIO196	196	GPIO197	197	GPIO198	198	GPIO199	199	
GPIO200	200	GPIO201	201	GPIO202	202	GPIO203	203	GPIO204	204	
GPIO205	205	GPIO206	206	GPIO207	207	GPIO208	208	GPIO209	209	
GPIO210	210	GPIO211	211	GPIO212	212	GPIO213	213	GPIO214	214	
GPIO215	215	GPIO216	216	GPIO217	217	GPIO218	218	GPIO219	219	
GPIO220	220	GPIO221	221	GPIO222	222	GPIO223	223	GPIO224	224	
GPIO225	225	GPIO226	226	GPIO227	227	GPIO228	228	GPIO229	229	
GPIO230	230	GPIO231	231	GPIO232	232	GPIO233	233	GPIO234	234	
GPIO235	235	GPIO236	236	GPIO237	237	GPIO238	238	GPIO239	239	
GPIO240	240	GPIO241	241	GPIO242	242	GPIO243	243	GPIO244	244	
GPIO245	245	GPIO246	246	GPIO247	247	GPIO248	248	GPIO249	249	
GPIO250	250	GPIO251	251	GPIO252	252	GPIO253	253	GPIO254	254	
GPIO255	255	GPIO256	256	GPIO257	257	GPIO258	258	GPIO259	259	
GPIO260	260	GPIO261	261	GPIO262	262	GPIO263	263	GPIO264	264	
GPIO265	265	GPIO266	266	GPIO267	267	GPIO268	268	GPIO269	269	
GPIO270	270	GPIO271	271	GPIO272	272	GPIO273	273	GPIO274	274	
GPIO275	275	GPIO276	276	GPIO277	277	GPIO278	278	GPIO279	279	
GPIO280	280	GPIO281	281	GPIO282	282	GPIO283	283	GPIO284	284	
GPIO285	285	GPIO286	286	GPIO287	287	GPIO288	288	GPIO289	289	
GPIO290	290	GPIO291	291	GPIO292	292	GPIO293	293	GPIO294	294	
GPIO295	295	GPIO296	296	GPIO297	297	GPIO298	298	GPIO299	299	
GPIO300	300	GPIO301	301	GPIO302	302	GPIO303	303	GPIO304	304	
GPIO305	305	GPIO306	306	GPIO307	307	GPIO308	308	GPIO309	309	
GPIO310	310	GPIO311	311	GPIO312	312	GPIO313	313	GPIO314	314	
GPIO315	315	GPIO316	316	GPIO317	317	GPIO318	318	GPIO319	319	
GPIO320	320	GPIO321	321	GPIO322	322	GPIO323	323	GPIO324	324	
GPIO325	325	GPIO326	326	GPIO327	327	GPIO328	328	GPIO329	329	
GPIO330	330	GPIO331	331	GPIO332	332	GPIO333	333	GPIO334	334	
GPIO335	335	GPIO336	336	GPIO337	337	GPIO338	338	GPIO339	339	
GPIO340	340	GPIO341	341	GPIO342	342	GPIO343	343	GPIO344	344	
GPIO345	345	GPIO346	346	GPIO347	347	GPIO348	348	GPIO349	349	
GPIO350	350	GPIO351	351	GPIO352	352	GPIO353	353	GPIO354	354	
GPIO355	355	GPIO356	356	GPIO357	357	GPIO358	358	GPIO359	359	
GPIO360	360	GPIO361	361	GPIO362	362	GPIO363	363	GPIO364	364	
GPIO365	365	GPIO366	366	GPIO367	367	GPIO368	368	GPIO369	369	
GPIO370	370	GPIO371	371	GPIO372	372	GPIO373	373	GPIO374	374	
GPIO375	375	GPIO376	376	GPIO377	377	GPIO378	378	GPIO379	379	
GPIO380	380	GPIO381	381	GPIO382	382	GPIO383	383	GPIO384	384	
GPIO385	385	GPIO386	386	GPIO387	387	GPIO388	388	GPIO389	389	
GPIO390	390	GPIO391	391	GPIO392	392	GPIO393	393	GPIO394	394	
GPIO395	395	GPIO396	396	GPIO397	397	GPIO398	398	GPIO399	399	
GPIO400	400	GPIO401	401	GPIO402	402	GPIO403	403	GPIO404	404	
GPIO405	405	GPIO406	406	GPIO407	407	GPIO408	408	GPIO409	409	
GPIO410	410	GPIO411	411	GPIO412	412	GPIO413	413	GPIO414	414	
GPIO415	415	GPIO416	416	GPIO417	417	GPIO418	418	GPIO419	419	
GPIO420	420	GPIO421	421	GPIO422	422	GPIO423	423	GPIO424	424	
GPIO425	425	GPIO426	426	GPIO427	427	GPIO428	428	GPIO429	429	
GPIO430	430	GPIO431	431	GPIO432	432	GPIO433	433	GPIO434	434	
GPIO435	435	GPIO436	436	GPIO437	437	GPIO438	438	GPIO439	439	
GPIO440	440	GPIO441	441	GPIO442	442	GPIO443	443	GPIO444	444	
GPIO445	445	GPIO446	446	GPIO447	447	GPIO448	448	GPIO449	449	
GPIO450	450	GPIO451	451	GPIO452	452	GPIO453	453	GPIO454	454	
GPIO455	455	GPIO456	456	GPIO457	457	GPIO458	458	GPIO459	459	
GPIO460	460	GPIO461	461	GPIO462	462	GPIO463	463	GPIO464	464	
GPIO465	465	GPIO466	466	GPIO467	467	GPIO468	468	GPIO469	469	
GPIO470	470	GPIO471	471	GPIO472	472	GPIO473	473	GPIO474	474	
GPIO475	475	GPIO476	476	GPIO477	477	GPIO478	478	GPIO479	479	
GPIO480	480	GPIO481	481	GPIO482	482	GPIO483	483	GPIO484	484	
GPIO485	485	GPIO486	486	GPIO487	487	GPIO488	488	GPIO489	489	
GPIO490	490	GPIO491	491	GPIO492	492	GPIO493	493	GPIO494	494	
GPIO495	495	GPIO496	496	GPIO497	497	GPIO498	498	GPIO499	499	
GPIO500	500	GPIO501	501	GPIO502	502	GPIO503	503	GPIO504	504	
GPIO505	505	GPIO506	506	GPIO507	507	GPIO508	508	GPIO509	509	
GPIO510	510	GPIO511	511	GPIO512	512	GPIO513	513	GPIO514	514	
GPIO515	515	GPIO516	516	GPIO517	517	GPIO518	518	GPIO519	519	
GPIO520	520	GPIO521	521	GPIO522	522	GPIO523	523	GPIO524	524	
GPIO525	525	GPIO526	526	GPIO527	527	GPIO528	528	GPIO529	529	
GPIO530	530	GPIO531	531	GPIO532	532	GPIO533	533	GPIO534	534	
GPIO535	535	GPIO536	536	GPIO537	537	GPIO538	538	GPIO539	539	
GPIO540	540	GPIO541	541	GPIO542	542	GPIO543	543	GPIO544	544	
GPIO545	545	GPIO546	546	GPIO547	547	GPIO548	548	GPIO549	549	
GPIO550	550	GPIO551	551	GPIO552	552	GPIO553	553	GPIO554	554	
GPIO555	555	GPIO556	556	GPIO557	557	GPIO558	558	GPIO559	559	
GPIO560	560	GPIO561	561	GPIO562	562	GPIO563	563	GPIO564	564	
GPIO565	565	GPIO566	566	GPIO567	567	GPIO568	568	GPIO569	569	
GPIO570	570	GPIO571	571	GPIO572	572	GPIO573	573	GPIO574	574	
GPIO575	575	GPIO576	576	GPIO577	577	GPIO578	578	GPIO579	579	
GPIO580	580	GPIO581	581	GPIO582	582	GPIO583	583	GPIO584	584	
GPIO585	585	GPIO586	586	GPIO587	587	GPIO588	588	GPIO589	589	
GPIO590	590	GPIO591	591	GPIO592	592	GPIO593	593	GPIO594	594	
GPIO595	595	GPIO596	596	GPIO597	597	GPIO598	598	GPIO599	599	
GPIO600	600	GPIO601	601	GPIO602	602	GPIO603	603	GPIO604	604	
GPIO605	605	GPIO606	606	GPIO607	607	GPIO608	608	GPIO609	609	
GPIO610	610	GPIO611	611	GPIO612	612	GPIO613	613	GPIO614	614	
GPIO615	615	GPIO616	616	GPIO617	617	GPIO618	618	GPIO619	619	
GPIO620	620	GPIO621	621	GPIO622	622	GPIO623	623	GPIO624	624	
GPIO625	625	GPIO626	626	GPIO627	627	GPIO628	628	GPIO629	629	
GPIO630	630	GPIO631	631	GPIO632	632	GPIO633	633	GPIO634	634	
GPIO635	635	GPIO636	636	GPIO637	637	GPIO638	638	GPIO639	639	
GPIO640	640	GPIO641	641	GPIO642	642	GPIO643	643	GPIO644	644	
GPIO645	645	GPIO646	646	GPIO647	647	GPIO648	648	GPIO649	649	
GPIO650	650	GPIO651	651	GPIO652	652	GPIO653	653	GPIO654	654	
GPIO655	655	GPIO656	656	GPIO657	657	GPIO658	658	GPIO659	659	
GPIO660	660	GPIO661	661	GPIO662	662	GPIO663	663	GPIO664	664	
GPIO665	665	GPIO666	666	GPIO667	667	GPIO668	668	GPIO669	669	
GPIO670	670	GPIO671	671	GPIO672	672	GPIO673	673	GPIO674	674	
GPIO675	675	GPIO676	676	GPIO677	677	GPIO678	678	GPIO679	679	
GPIO680	680	GPIO681	681	GPIO682	682	GPIO683	683	GPIO684	684	
GPIO685	685	GPIO686	686	GPIO687	687	GPIO688	688	GPIO689	689	
GPIO690	690	GPIO691	691	GPIO692	692	GPIO693	693	GPIO694	694	
GPIO695	695	GPIO696	696	GPIO697	697	GPIO698	698	GPIO699	699	
GPIO700	700									

[illegible]

G3

3V ADAPTER

+19V_DCBATOUT

+3D3V_DSW (PCH) (EC)

PR4529

+3D3V_DSW_1

+3D3V_EN2

PWM

PI4501
RT6576DGQW2-GP

PAD

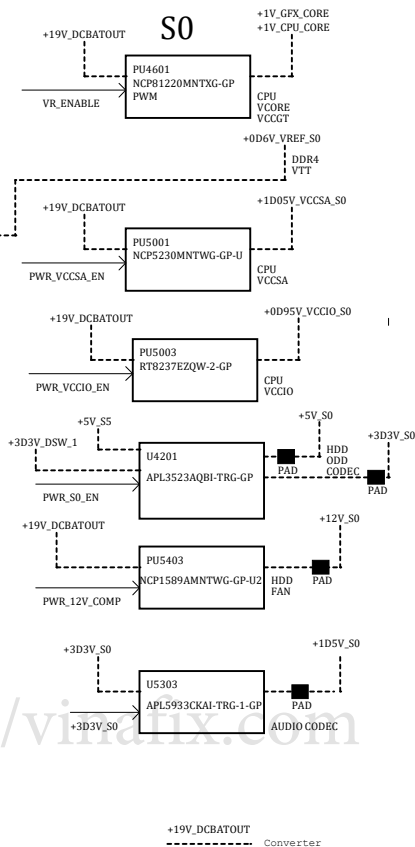
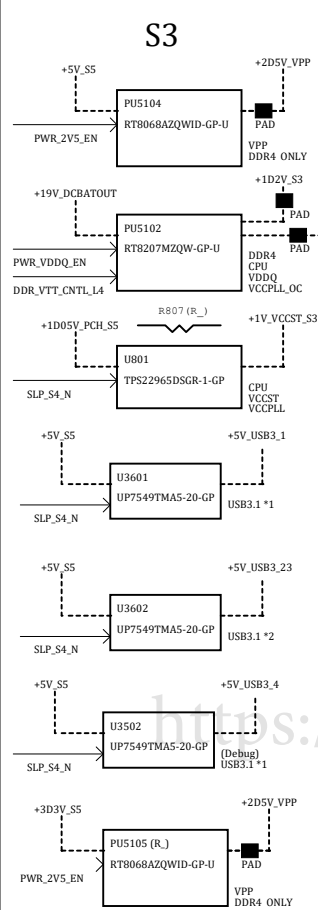
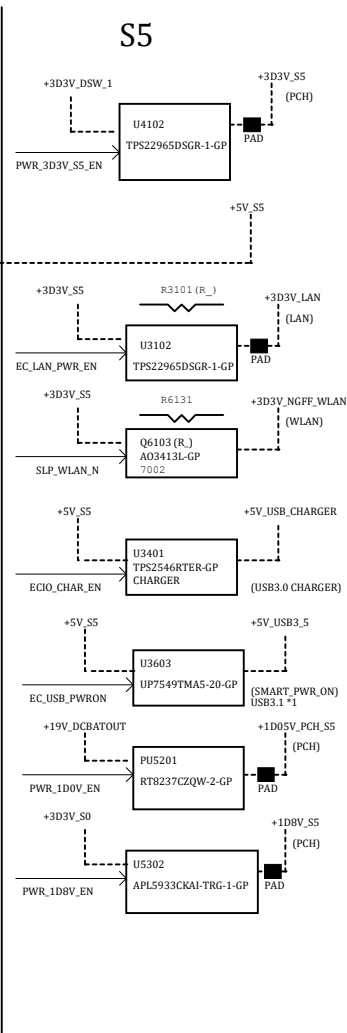
PAD

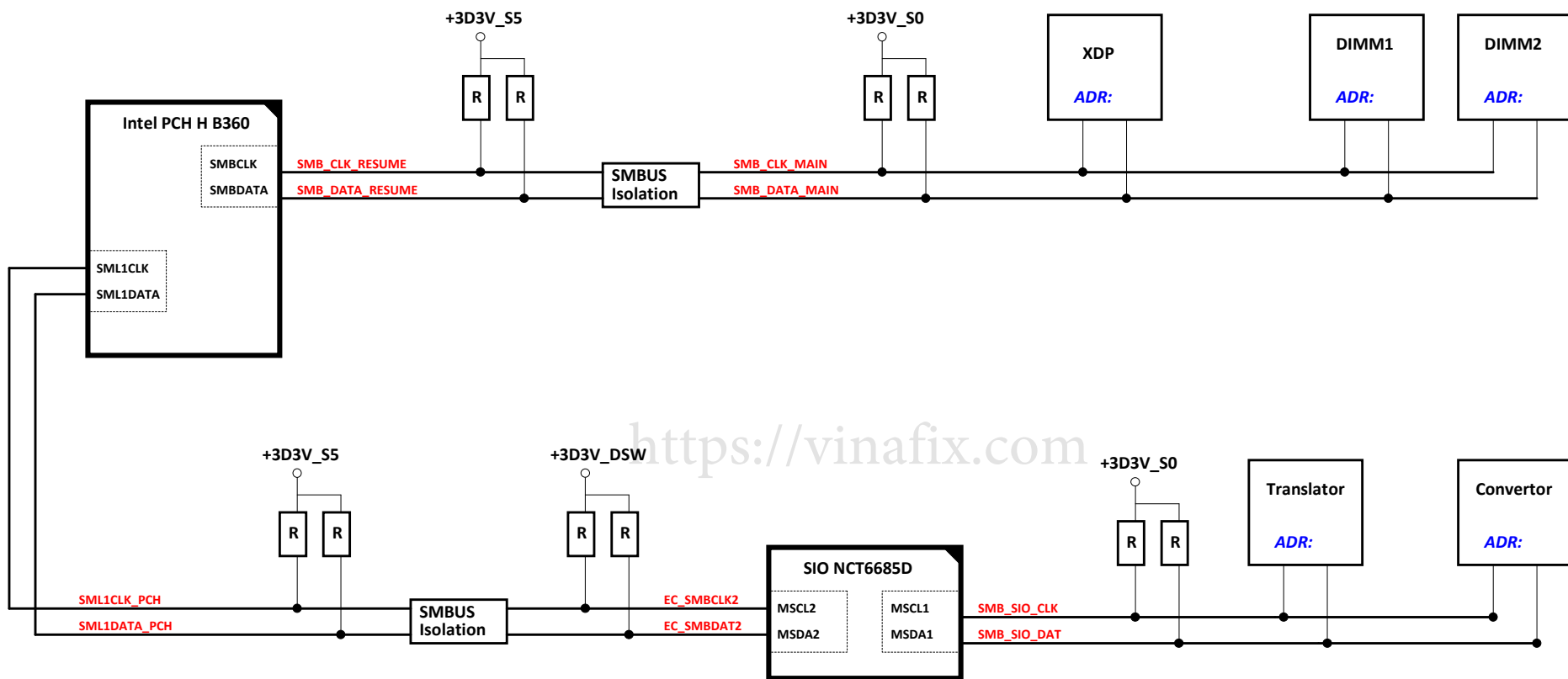
+3D3V_DSW

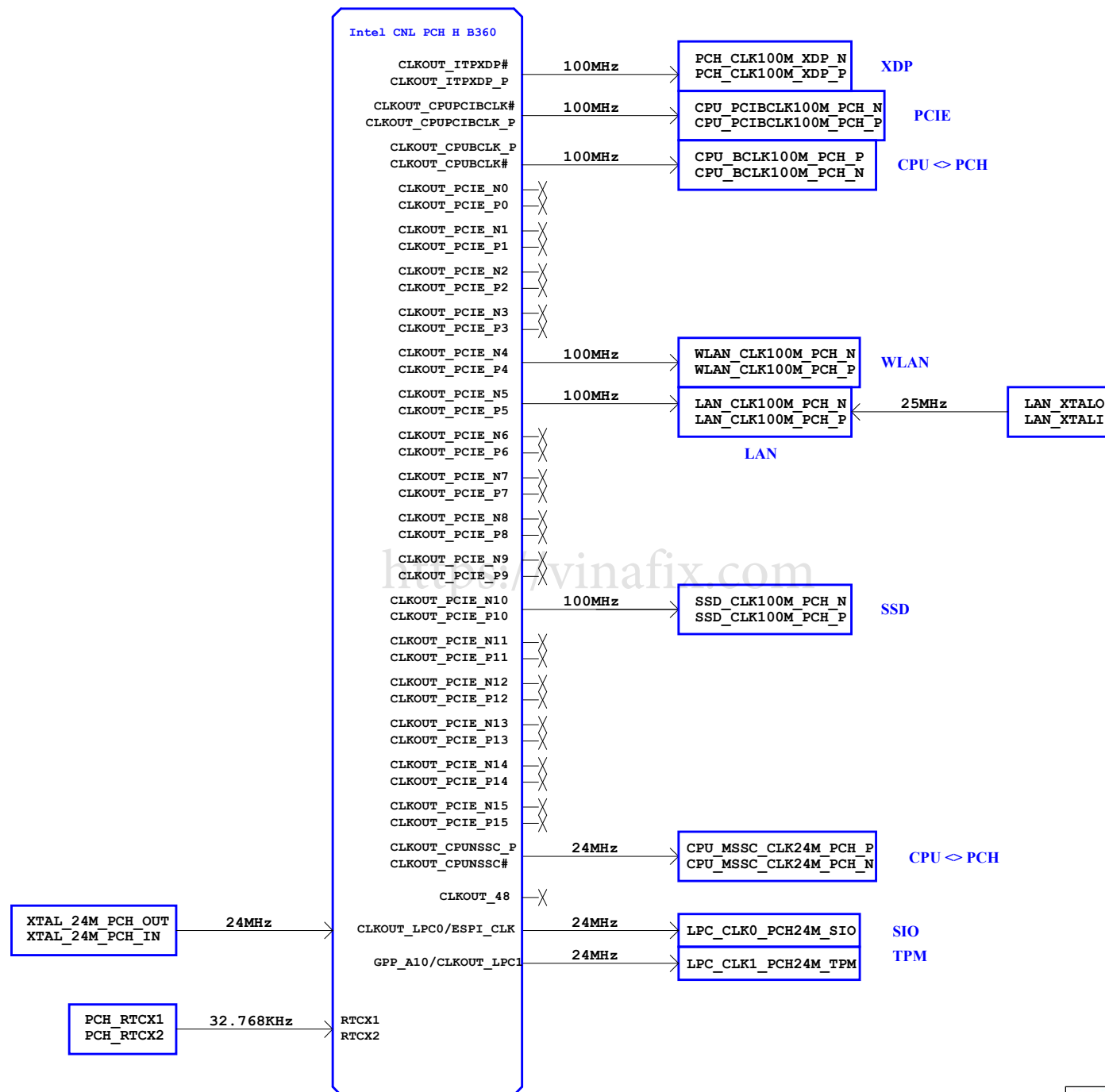
BATTERY

+3V_RTC


D2501

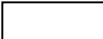








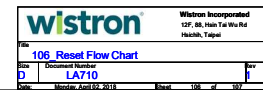
NOTE:


CHIP or Circuit


SOCKET or SLOT or CON



Resistor


Logic gate or behavior



A710 / V330 SB

1. Unmount R9513 / R9511 for EC combine PS8625 FW
2. Remove U9504 R9533 R9534 R9536 C9530 for EC combine PS8625 FW
3. Remove U9505 R9502 R9503 R9504 for BIOS combine PS8625 EDID
4. Change R3408 to 22K (64.22025.6DL) => Change USB Charger I_{max} setting to 2.2A
5. Change C802 to 2200pF (78.22224.2FLLL) => Fix +1V VCCST S3 rising time to short issue.
6. Add C805 0.1uF (78.10421.2FLLL) near C803 => Fix +1V VCCST S3 V_{max} over spec issue.
7. Change C4208, C4209 to 1uF (78.10523.5FLLL) => Fix +5V S5 to +5V S0 V_{drop} over spec issue.
8. Mount R429 to 0R (63.10234.1DL) / Unmount R430 => Fix TRST can't install issue.
9. Replace L2402 to R2466 => 2.2R / F / 0603 (64.2R205.55L) => Fix +3D3V AUX SIO analog power noise (1M~10M) >30mV issue.
10. Change R2723 to 2.2R / F / 0603 (64.2R205.55L) => Fix +5V CODEC analog power noise (1M~10M) >30mV issue.
11. Mount C4001 to 0.1uF (78.10421.2FLLL) ; Change R4045 from 22K to 10K (63.10334.1DL)
=> Fix VR_EN to VR_READY over 2.5ms issue.
12. Add C1701 to 15pF (78.15034.1FLLL) => Fix PLTRST CPU_N overshoot issue.
13. Add C2009 to 15pF (78.15034.1FLLL) => Fix H_PWRGD overshoot issue.
14. Change R4404 to 3K (64.30015.6DL) => Setting Power Meter ilimit=6A(120W)
15. Change q9101 pin G to +5V S0 => Fix LPC_RST SIO V_{max} issue.
16. Change BTT2 -> 23.20023.001 => Change coin battery vendor to Maxell.
17. Add EC4201 / EC4202 => 0.1uF (78.10421.2FLLL) => EMC request for +5V S0.
18. Mount C3122 to 4.7uF (78.47520.5BLLL) / C3128 to 2.2uF (78.22523.5BLLL) ;
Add EC3201=> 0.1uF (78.10421.2FLLL) => 0.1uF (78.10421.2FLLL) => EMC request for +3D3V_LAN.
19. Add R3804 R3806 R3805 R3808 for Smart Power on option
20. Add R3807 R3810 R3809 R3811 for Non-Smart Power on option
21. Change R3603 to 100K (63.10434.1DL) Add R2464 to 0R (63.R0034.1DL) => Add SMARTPWR_EN control USB Smart Power On
22. Add C1902 to 68pF (78.68034.1FLLL) => Fix LPC_AD SIO P0 Ring up and Ring down warning
23. Add R6118 R6120 to 10R (64.10R05.6DL) => Fix WLAN USB eye diagram issue.
24. Add R2401 , unmount R2017 => For EC ME_UNLOCK_N to control ME Disable / Enable
25. Mount R2065 => Fix if G3 to Deep S5, SLP_SUS_N have high/low level cycle issue.

		Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title 107_Change History			
Size B	Document Number LA710		Rev 1
Date:	Monday, April 02, 2018		Sheet 107 of 107